- **Low Supply-Voltage Range, 1.8 V . . . 3.6 V**
- **Ultralow-Power Consumption:**
  - **Active Mode: 280 μA at 1 MHz, 2.2 V**
  - **Standby Mode: 1.6 μA**
  - **RAM Retention Off Mode: 0.1 μA**
- **Five Power-Saving Modes**
- **Wake-Up From Standby Mode in 6 μs**
- **16-Bit RISC Architecture, 125-ns Instruction Cycle Time**
- **Three-Channel Internal DMA**
- **12-Bit A/D Converter With Internal Reference, Sample-and-Hold and Autoscan Feature**
- **Dual 12-Bit D/A Converters With Synchronization**
- **16-Bit Timer With Seven Capture/Compare-With-Shadow Registers, Timer_B**
- **16-Bit Timer With Three Capture/Compare Registers, Timer_A**
- **On-Chip Comparator**
- **Serial Onboard Programming**
- **Programmable Code Protection by Security Fuse**
- **Bootstrap Loader**
- **Serial Communication Interface (USART1), Functions as Asynchronous UART or Synchronous Interface**
- **Serial Communication Interface (USART0), Functions as Asynchronous UART or Synchronous SPI or I^2C Interface**
- **Brownout Detector**
- **Supply Voltage Supervisor/Monitor With Programmable Level Detection**
- **Family Members Include:**
  - **MSP430F155:**
    16KB+256B Flash Memory
    512B RAM
  - **MSP430F156**
    24KB+256B Flash Memory
    512B RAM
  - **MSP430F157**
    32KB+256B Flash Memory
    1KB RAM
  - **MSP430F167:**
    32KB+256B Flash Memory,
    1KB RAM
  - **MSP430F168:**
    48KB+256B Flash Memory,
    2KB RAM
  - **MSP430F169:**
    60KB+256B Flash Memory,
    2KB RAM
- **Available in 64-Pin Quad Flat Pack (QFP)**
- **For Complete Module Descriptions, See the *MSP430x1xx Family User's Guide*, Literature Number SLAU049**

PRODUCT PREVIEW

description

The Texas Instruments MSP430 series is an ultralow-power microcontroller family consisting of several devices featuring different sets of modules targeted to various applications. The microcontroller is designed to be battery operated for use in extended-time applications. The MSP430 achieves maximum code efficiency with its 16-bit RISC architecture, 16-bit CPU-integrated registers, and a constant generator. The digitally-controlled oscillator provides wake-up from low-power mode to active mode in less than 6 μs. The MSP430x16x series are microcontroller configurations with two built-in 16-bit timers, a fast 12-bit A/D converter, dual 12-bit D/A converter, two universal serial synchronous/asynchronous communication interfaces (USART), I^2C, DMA, and 48 I/O pins.

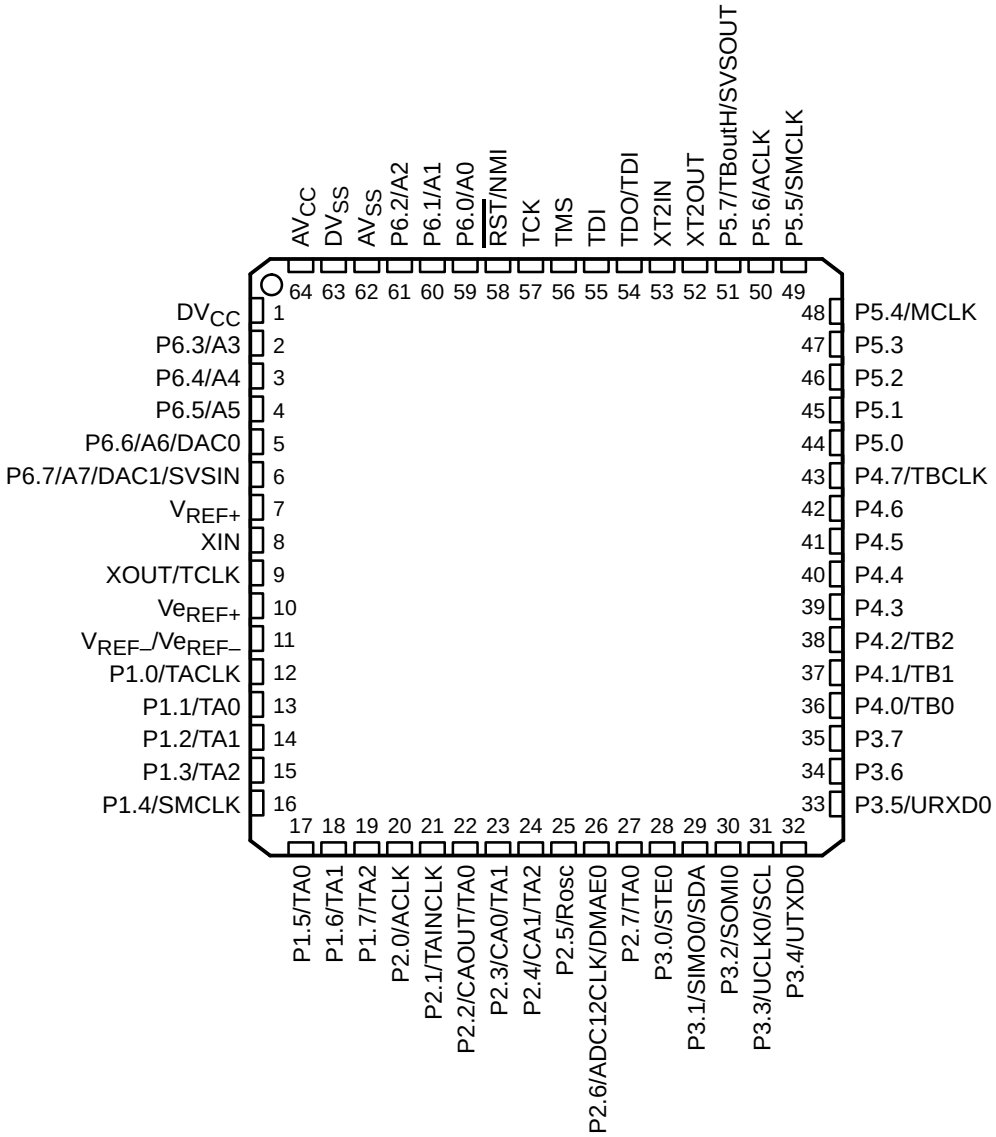
Typical applications include sensor systems that capture analog signals, convert them to digital values, and process and transmit the data to a host system. The timers make the configurations ideal for industrial control applications such as digital motor control, hand-held meters, TEC control in optical networks, etc. The hardware multiplier enhances the performance and offers a broad code and hardware-compatible family solution.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES
	PLASTIC 64-PIN QFP (PM)
–40°C to 85°C	MSP430F155IPM MSP430F156IPM MSP430F157IPM MSP430F167IPM MSP430F168IPM MSP430F169IPM

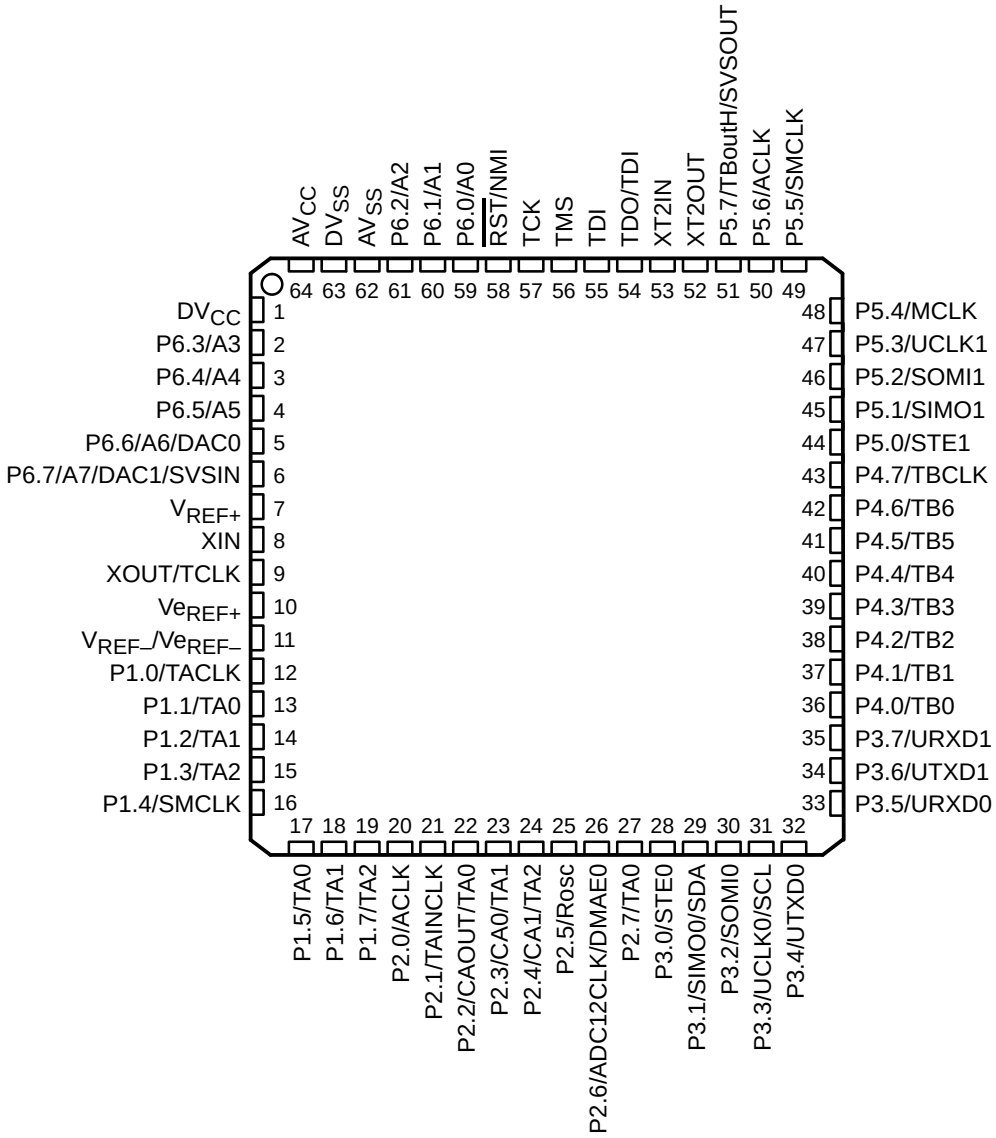
pin designation, MSP430F155, MSP430F156, and MSP430F157

PM PACKAGE
(TOP VIEW)



pin designation, MSP430F167, MSP430F168, MSP430F169

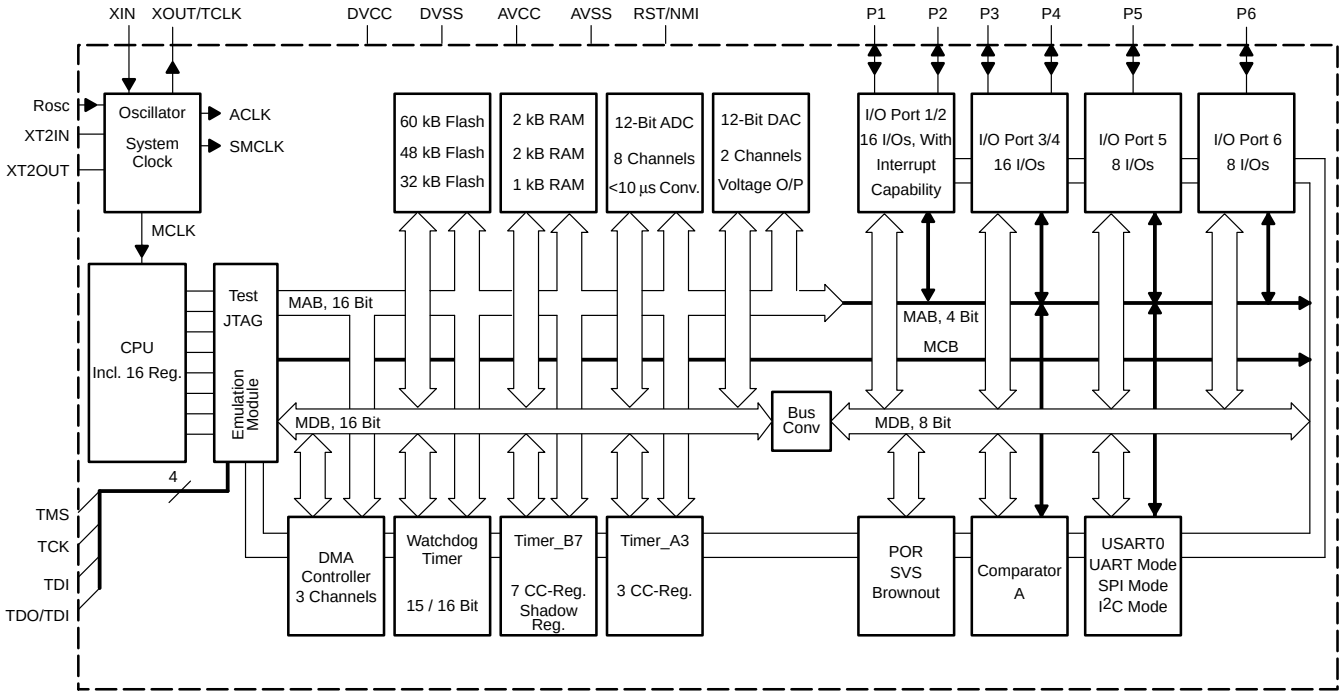
PM PACKAGE
(TOP VIEW)



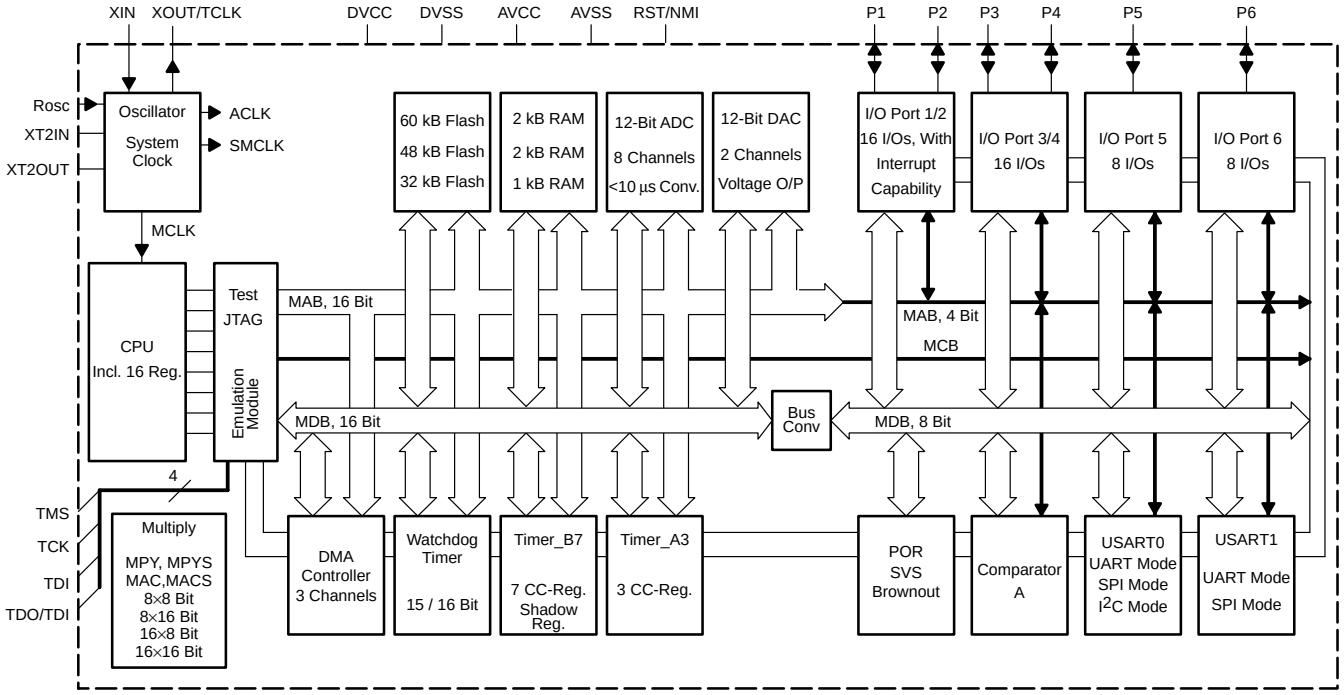
PRODUCT PREVIEW

functional block diagrams

MSP430x15x



MSP430x16x



PRODUCT PREVIEW

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AV_{CC}	64		Analog supply voltage, positive terminal. Supplies only the analog portion of ADC12 and DAC12.
AV_{SS}	62		Analog supply voltage, negative terminal. Supplies only the analog portion of ADC12 and DAC12.
DV_{CC}	1		Digital supply voltage, positive terminal. Supplies all digital parts.
DV_{SS}	63		Digital supply voltage, negative terminal. Supplies all digital parts.
P1.0/TACLK	12	I/O	General-purpose digital I/O pin/Timer_A, clock signal TACLK input
P1.1/TA0	13	I/O	General-purpose digital I/O pin/Timer_A, capture: CCI0A input, compare: Out0 output
P1.2/TA1	14	I/O	General-purpose digital I/O pin/Timer_A, capture: CCI1A input, compare: Out1 output
P1.3/TA2	15	I/O	General-purpose digital I/O pin/Timer_A, capture: CCI2A input, compare: Out2 output
P1.4/SMCLK	16	I/O	General-purpose digital I/O pin/SMCLK signal output
P1.5/TA0	17	I/O	General-purpose digital I/O pin/Timer_A, compare: Out0 output
P1.6/TA1	18	I/O	General-purpose digital I/O pin/Timer_A, compare: Out1 output
P1.7/TA2	19	I/O	General-purpose digital I/O pin/Timer_A, compare: Out2 output/
P2.0/ACLK	20	I/O	General-purpose digital I/O pin/ACLK output
P2.1/TAINCLK	21	I/O	General-purpose digital I/O pin/Timer_A, clock signal at INCLK
P2.2/CAOUT/TA0	22	I/O	General-purpose digital I/O pin/Timer_A, capture: CCI0B input/Comparator_A output
P2.3/CA0/TA1	23	I/O	General-purpose digital I/O pin/Timer_A, compare: Out1 output/Comparator_A input
P2.4/CA1/TA2	24	I/O	General-purpose digital I/O pin/Timer_A, compare: Out2 output/Comparator_A input
P2.5/Rosc	25	I/O	General-purpose digital I/O pin, input for external resistor defining the DCO nominal frequency
P2.6/ADC12CLK/ DMAE0	26	I/O	General-purpose digital I/O pin, conversion clock – 12-bit ADC, DMA channel 0 external trigger
P2.7/TA0	27	I/O	General-purpose digital I/O pin/Timer_A, compare: Out0 output
P3.0/STE0	28	I/O	General-purpose digital I/O, slave transmit enable – USART0/SPI mode
P3.1/SIMO0/SDA	29	I/O	General-purpose digital I/O, slave in/master out of USART0/SPI mode, I^2C data – USART0/I^2C mode
P3.2/SOMI0	30	I/O	General-purpose digital I/O, slave out/master in of USART0/SPI mode
P3.3/UCLK0/SCL	31	I/O	General-purpose digital I/O, external clock input – USART0/UART or SPI mode, clock output – USART0/SPI mode, I^2C clock – USART0/I^2C mode
P3.4/UTXD0	32	I/O	General-purpose digital I/O, transmit data out – USART0/UART mode
P3.5/URXD0	33	I/O	General-purpose digital I/O, receive data in – USART0/UART mode
P3.6/UTXD1†	34	I/O	General-purpose digital I/O, transmit data out – USI1/UART mode
P3.7/URXD1†	35	I/O	General-purpose digital I/O, receive data in – USI1/UART mode
P4.0/TB0	36	I/O	General-purpose digital I/O, capture I/P or PWM output port – Timer_B7 CCR0
P4.1/TB1	37	I/O	General-purpose digital I/O, capture I/P or PWM output port – Timer_B7 CCR1
P4.2/TB2	38	I/O	General-purpose digital I/O, capture I/P or PWM output port – Timer_B7 CCR2
P4.3/TB3†	39	I/O	General-purpose digital I/O, capture I/P or PWM output port – Timer_B7 CCR3
P4.4/TB4†	40	I/O	General-purpose digital I/O, capture I/P or PWM output port – Timer_B7 CCR4
P4.5/TB5†	41	I/O	General-purpose digital I/O, capture I/P or PWM output port – Timer_B7 CCR5
P4.6/TB6†	42	I/O	General-purpose digital I/O, capture I/P or PWM output port – Timer_B7 CCR6
P4.7/TBCLK	43	I/O	General-purpose digital I/O, input clock TBCLK – Timer_B7
P5.0/STE1†	44	I/O	General-purpose digital I/O, slave transmit enable – USART1/SPI mode
P5.1/SIMO1†	45	I/O	General-purpose digital I/O slave in/master out of USART1/SPI mode
P5.2/SOMI1†	46	I/O	General-purpose digital I/O, slave out/master in of USART1/SPI mode
P5.3/UCLK1†	47	I/O	General-purpose digital I/O, external clock input – USART1/UART or SPI mode, clock output – USART1/SPI mode

† 16x devices only

PRODUCT PREVIEW

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
P5.4/MCLK	48	I/O	General-purpose digital I/O, main system clock MCLK output
P5.5/SMCLK	49	I/O	General-purpose digital I/O, submain system clock SMCLK output
P5.6/ACLK	50	I/O	General-purpose digital I/O, auxiliary clock ACLK output
P5.7/TBoutH/ SVSOUT	51	I/O	General-purpose digital I/O, switch all PWM digital output ports to high impedance – Timer_B7 TB0 to TB6, SVS comparator output
P6.0/A0	59	I/O	General-purpose digital I/O, analog input a0 – 12-bit ADC
P6.1/A1	60	I/O	General-purpose digital I/O, analog input a1 – 12-bit ADC
P6.2/A2	61	I/O	General-purpose digital I/O, analog input a2 – 12-bit ADC
P6.3/A3	2	I/O	General-purpose digital I/O, analog input a3 – 12-bit ADC
P6.4/A4	3	I/O	General-purpose digital I/O, analog input a4 – 12-bit ADC
P6.5/A5	4	I/O	General-purpose digital I/O, analog input a5 – 12-bit ADC
P6.6/A6/DAC0	5	I/O	General-purpose digital I/O, analog input a6 – 12-bit ADC, DAC12.0 output
P6.7/A7/DAC1/ SVSIN	6	I/O	General-purpose digital I/O, analog input a7 – 12-bit ADC, DAC12.1 output, SVS input
$\overline{\text{RST}}$/NMI	58	I	Reset input, nonmaskable interrupt input port, or bootstrap loader start (in Flash devices).
TCK	57	I	Test clock. TCK is the clock input port for device programming test and bootstrap loader start
TDI	55	I	Test data input. TDI is used as a data input port. The device protection fuse is connected to TDI.
TDO/TDI	54	I/O	Test data output port. TDO/TDI data output or programming data input terminal
TMS	56	I	Test mode select. TMS is used as an input port for device programming and test.
V_{eREF+}	10	I/P	Input for an external reference voltage
V_{REF+}	7	O	Output of positive terminal of the reference voltage in the ADC12
V_{REF-}/V_{eREF-}	11	O	Negative terminal for the reference voltage for both sources, the internal reference voltage, or an external applied reference voltage
XIN	8	I	Input port for crystal oscillator XT1. Standard or watch crystals can be connected.
XOUT/TCLK	9	I/O	Output terminal of crystal oscillator XT1 or test clock input
XT2IN	53	I	Input port for crystal oscillator XT2. Only standard crystals can be connected.
XT2OUT	52	O	Output terminal of crystal oscillator XT2

PRODUCT PREVIEW

short-form description

processing unit

The processing unit is based on a consistent and orthogonal CPU and instruction set. This design structure results in a RISC-like architecture, highly transparent to the application development and notable for its ease of programming. All operations other than program-flow instructions are consequently performed as register operations in conjunction with seven addressing modes for source and four modes for destination operand.

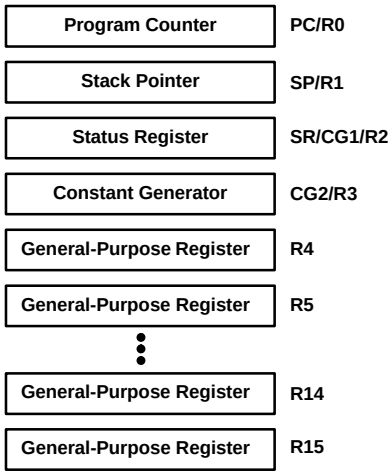
short-form description (continued)

CPU

The CPU has sixteen registers that provide reduced instruction execution time. This reduces the register-to-register operation execution time to one cycle of the processor frequency.

Four of the registers are reserved for special use as program counter, stack pointer, status register, and constant generator. The remaining registers are available as general-purpose registers.

Peripherals are connected to the CPU using a data address and control bus, and can be easily handled with all memory manipulation instructions.



instruction set

The instruction set for this register-to-register architecture constitutes a powerful and easy-to-use assembler language. The instruction set consists of 51 instructions with three formats and seven address modes. Table 1 provides a summary and example of the three types of instruction formats; the address modes are listed in Table 2.

Table 1. Instruction Word Formats

Dual operands, source-destination	e.g. ADD R4,R5	R4 + R5 ——> R5
Single operands, destination only	e.g. CALL R8	PC —>(TOS), R8—> PC
Relative jump, un/conditional	e.g. JNE	Jump-on-equal bit = 0

Each instruction operating on word and byte data is identified by the suffix B.

Examples:	WORD INSTRUCTIONS		BYTE INSTRUCTIONS	
	MOV	EDE, TONI	MOV.B	EDE,TONI
	ADD	#235h,&MEM	ADD.B	#35h,&MEM
	PUSH	R5	PUSH.B	R5
	SWPB	R5	—	

Table 2. Address Mode Descriptions

ADDRESS MODE	S	D	SYNTAX	EXAMPLE	OPERATION
Register	✓	✓	MOV Rs,Rd	MOV R10,R11	R10 —> R11
Indexed	✓	✓	MOV X(Rn),Y(Rm)	MOV 2(R5),6(R6)	M(2+R5)—> M(6+R6)
Symbolic (PC relative)	✓	✓	MOV EDE,TONI		M(EDE) —> M(TONI)
Absolute	✓	✓	MOV &MEM,&TCDAT		M(MEM) —> M(TCDAT)
Indirect	✓		MOV @Rn,Y(Rm)	MOV @R10,Tab(R6)	M(R10) —> M(Tab+R6)
Indirect autoincrement	✓		MOV @Rn+,Rm	MOV @R10+,R11	M(R10) —> R11 R10 + 2—> R10
Immediate	✓		MOV #X,TONI	MOV #45,TONI	#45 —> M(TONI)

NOTE: S = source D = destination

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Computed branches (BR) and subroutine call (CALL) instructions use the same address modes as other instructions. These address modes provide *indirect* addressing, which is ideally suited for computed branches and calls. The full use of this programming capability results in a program structure which is different from structures used with conventional 8- and 16-bit controllers. For example, numerous routines can be easily designed to deal with pointers and stacks instead of using flag-type programs for flow control.

operating modes and interrupts

The MSP430 operating modes provide advanced support of the requirements for ultralow-power and ultralow-energy consumption. This goal is achieved by intelligent management during the different operating modes of modules and CPU states and is fully supported during interrupt event handling. An interrupt event awakes the system from each of the various operating modes and returns, using the *RETI* instruction, to the mode that was selected before the interrupt event occurred. The different requirements on CPU and modules—driven by system cost and current consumption objectives—require the use of different clock signals:

- Auxiliary clock ACLK, sourced by LFXT1CLK (crystal frequency) and used by the peripheral modules
- Main system clock MCLK, used by the CPU and system
- Subsystem clock SMCLK, used by the peripheral modules

low-power consumption capabilities

The various operating modes are handled by software by controlling the operation of the internal clock system. This clock system provides a large combination of hardware and software capabilities to run the application while maintaining the lowest power consumption and optimizing system costs. This is accomplished by:

- Use of the internal clock (DCO) generator without any external components
- Selection of an external crystal or ceramic resonator for lowest frequency and cost
- Selection and activation of the proper clock signals (LFXT1CLK, XT2Off, and/or DCOCLK) and clock predivider function. Control bit XT2Off is embedded in control register BCSCTL1.
- Application of an external clock source

The control bits that most influence the operation of the clock system and support fast turnon from low power operating modes are located in the status register SR. Four bits control the CPU and the system clock generator: SCG1, SCG0, OscOff, and CPUOff.

15 … 9	8	7							0
Reserved For Future Enhancements	V	SCG1	SCG0	OscOff	CPUOff	GIE	N	Z	C
rw-0									

CPUOff, SCG1, SCG0, and OscOff are the most important bits in low-power control when the basic function of the system clock generator is established. They are pushed to the stack whenever an interrupt is accepted and saved for returning to the operation before an interrupt request. They can be manipulated via indirect access to the data on the stack during execution of an interrupt handler so that program execution can resume in another power operating mode after return-from-interrupt.

CPUOff: Clock signal MCLK, used with the CPU, is active when the CPUOff bit is reset or stopped when set.

SCG1: Clock signal SMCLK, used with peripherals, is enabled when the SCG1 bit is reset or stopped when set.

OscOff: Crystal oscillator LFXT1 is active when the OscOff bit is reset. The LFXT1 oscillator can be inactive only when the OscOff bit is set and it is not used for MCLK. The setup time to start a crystal oscillation requires special consideration when the off option is used. Mask-programmable devices can disable this feature and the oscillator can never be switched off by software.

SCG0: The dc generator is active when the SCG0 bit is reset. The DCO can be inactive only if the SCG0 bit is set and the DCOCLK signal is not used as MCLK or SMCLK. The dc current consumed by the dc generator defines the basic frequency of the DCOCLK.

When the current is switched off (SCG0=1) the start of the DCOCLK is slightly delayed. This delay is in the microsecond range.

DCOCLK: Clock signal DCOCLK is stopped if not used as MCLK or SMCLK. There are two situations when the SCG0 bit can not switch the DCOCLK signal off:

The DCOCLK frequency is used as MCLK (CPUOff=0 and SELM.1=0), or the DCOCLK frequency is used as SMCLK (SCG1=0 and SELS=0).

If DCOCLK is required for operation, the SCG0 bit can not switch the dc generator off.

interrupt vector addresses

The interrupt vectors and the power-up starting address are located in the address range 0FFFFh – 0FFE0h. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-up External Reset Watchdog Flash memory	WDTIFG KEYV (see Note 1)	Reset	0FFFEh	15, highest
NMI Oscillator Fault Flash memory access violation	NMIIFG (see Notes 1 & 4) OFIFG (see Notes 1 & 4) ACCVIFG (see Notes 1 & 4)	(Non)maskable (Non)maskable (Non)maskable	0FFFCh	14
Timer_B7 (see Note 5)	BCCIFG0 (see Note 2)	Maskable	0FFFAh	13
Timer_B7 (see Note 5)	BCCIFG1 to BCCIFG6 TBIFG (see Notes 1 & 2)	Maskable	0FFF8h	12
Comparator_A	CAIFG	Maskable	0FFF6h	11
Watchdog timer	WDTIFG	Maskable	0FFF4h	10
USART0 receive I2C transmit/receive/others	URXIFG0 I2CIFG (see Note 5)	Maskable	0FFF2h	9
USART0 transmit	UTXIFG0	Maskable	0FFF0h	8
ADC	ADCIFG (see Notes 1 & 2)	Maskable	0FFEEh	7
Timer_A3	CCIFG0 (see Note 2)	Maskable	0FFECh	6
Timer_A3	CCIFG1, CCIFG2, TAIFG (see Notes 1 & 2)	Maskable	0FFEAh	5
I/O port P1 (eight flags)	P1IFG.0 (see Notes 1 & 2) To P1IFG.7 (see Notes 1 & 2)	Maskable	0FFE8h	4
USART1 receive	URXIFG1	Maskable	0FFE6h	3
USART1 transmit	UTXIFG1	Maskable	0FFE4h	2
I/O port P2 (eight flags)	P2IFG.0 (see Notes 1 & 2) To P2IFG.7 (see Notes 1 & 2)	Maskable	0FFE2h	1
DAC12 DMA	DAC12.0IFG, DAC12.1IFG DMA0IFG, DMA1IFG, DMA2IFG (see Notes 1 & 2)	Maskable	0FFE0h	0, lowest

NOTES: 1. Multiple source flags
2. Interrupt flags are located in the module.
3. (Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general-interrupt enable cannot disable it.
4. Timer_B7 in MSP430x16x family has 7 CCRs; Timer_B3 in MSP430x15x family has 3 CCRs; in Timer_B3 there are only interrupt flags CCIFG0, 1, and 2, and the interrupt-enable bits CCIE0, 1, and 2 integrated.
5. I2C interrupt flags located in the module

special function registers

Most interrupt and module-enable bits are collected in the lowest address space. Special-function register bits not allocated to a functional purpose are not physically present in the device. This arrangement provides simple software access.

interrupt enable 1 and 2

Address	7	6	5	4	3	2	1	0
0h	UTXIE0	URXIE0	ACCVIE	NMIIE			OFIE	WDTIE
	rw-0	rw-0	rw-0	rw-0			rw-0	rw-0

WDTIE: Watchdog timer interrupt enable. Inactive if watchdog mode is selected. Active if watchdog timer is configured as general-purpose timer.

OFIE: Oscillator-fault-interrupt enable

NMIIE: Nonmaskable-interrupt enable

ACCVIE: Flash memory access viloation interrupt enable

URXIE0: USART0, UART, and SPI receive-interrupt enable

UTXIE0: USART0, UART, and SPI transmit-interrupt enable

Address	7	6	5	4	3	2	1	0
01h			UTXIE1	URXIE1				
			rw-0	rw-0				

URXIE1†: USART1, UART, and SPI receive-interrupt enable

UTXIE1†: USART1, UART, and SPI transmit-interrupt enable

† URXIE1 and UTXIE1 are not present in MSP430F15x devices.

interrupt flag register 1 and 2

Address	7	6	5	4	3	2	1	0
02h	UTXIFG0	URXIFG0		NMIIFG			OFIFG	WDTIFG
	rw-1	rw-0		rw-0			rw-1	rw-0

WDTIFG: Set on watchdog-timer overflow (in watchdog mode) or security key violation
Reset on VCC power-on, or a reset condition at the $\overline{\text{RST}}$/NMI pin in reset mode

OFIFG: Flag set on oscillator fault

NMIIFG: Set via $\overline{\text{RST}}$/NMI pin

URXIFG0: USART0, UART, and SPI receive flag

UTXIFG0: USART0, UART, and SPI transmit flag

Address	7	6	5	4	3	2	1	0
03h			UTXIFG1	URXIFG1				
			rw-1	rw-0				

URXIFG1‡: USART1, UART, and SPI receive flag

UTXIFG1‡: USART1, UART, and SPI transmit flag

‡ URXIFG1 and UTXIFG1 are not present in MSP430F15x devices.

PRODUCT PREVIEW

module enable registers 1 and 2

Address	7	6	5	4	3	2	1	0
04h	UTXE0	URXE0 USPIE0						
	rw-0	rw-0						

URXE0: USART0, UART mode receive enable

UTXE0: USART0, UART mode transmit enable

USPIE0: USART0, SPI mode transmit and receive enable

Address	7	6	5	4	3	2	1	0
05h			UTXE1	URXE1 USPIE1				
			rw-0	rw-0				

URXE1†: USART1, UART mode receive enable

UTXE1†: USART1, UART mode transmit enable

USPIE1†: USART1, SPI mode transmit and receive enable

† URXE1, UTXE1, and USPIE1 are not present in MSP430F15x devices.

Legend: rw: **Bit Can Be Read and Written**
rw-0: **Bit Can Be Read and Written. It Is Reset by PUC.**
SFR Bit Not Present in Device

memory organization

		MSP430F167	MSP430F168	MSP430F169
Memory Main: interrupt vector Main: code memory	Size Flash Flash	32kB 0FFFFh – 0FFE0h 0FFFFh – 08000h	48kB 0FFFFh – 0FFE0h 0FFFFh – 04000h	60kB 0FFFFh – 0FFE0h 0FFFFh – 01100h
Information memory	Size Flash	256 Byte 010FFh – 01000h	256 Byte 010FFh – 01000h	256 Byte 010FFh – 01000h
Boot memory	Size ROM	1kB 0FFFh – 0C00h	1kB 0FFFh – 0C00h	1kB 0FFFh – 0C00h
RAM	Size	1kB 05FFh – 0200h	2kB 09FFh – 0200h	2kB 09FFh – 0200h
Peripherals	16-bit 8-bit 8-bit SFR	01FFh – 0100h 0FFh – 010h 0Fh – 00h	01FFh – 0100h 0FFh – 010h 0Fh – 00h	01FFh – 0100h 0FFh – 010h 0Fh – 00h

boot ROM containing bootstrap loader

The intention of the bootstrap loader is to download data into the flash memory module. Various write, read, and erase operations are needed for a proper download environment. The bootstrap loader is only available on flash-memory devices.

functions of the bootstrap loader:

Definition of read: Apply and transmit data of peripheral registers or memory to pin P1.1 (BSLTX)
write: Read data from pin P2.2 (BSLRX) and write them into flash memory

boot ROM containing bootstrap loader (continued)

unprotected functions

Mass erase, erase of the main memory (segment 0 to segment n) and information memory (segment A and segment B)
Access to the MSP430 via the bootstrap loader is protected. It must be enabled before any protected function can be performed. The 256 bits in 0FFE0h to 0FFFFh provide the access key.

protected functions

All protected functions can be executed only if the access is enabled.

- Write/program byte into flash memory; parameters passed are start address and number of bytes (the segment-write feature of the flash memory is not supported and not useful with the UART protocol).
- Segment erase of segment 0 to segment n in main memory, and segment erase of segments A and B in the information memory.
- Read all data in main memory and information memory.
- Read and write to all byte peripheral modules and RAM.
- Modify PC and start program execution immediately.

NOTE:

Unauthorized readout of code and data is prevented by the user's definition of the data in the interrupt memory locations.

boot ROM containing bootstrap loader (continued)

features of the bootstrap loader are:

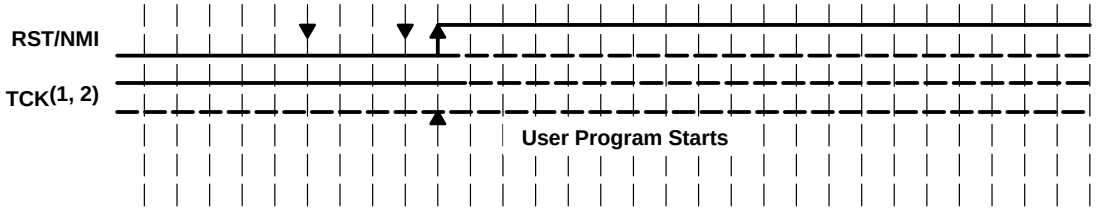
- UART communication protocol, fixed to 9600 baud
- Port pin P1.1 for transmit, P2.2 for receive
- TI standard serial protocol definition
- Implemented in flash memory version only
- Program execution starts with the user vector at 0FFFEh or with the bootstrap loader (start vector is at address 0C00h)

hardware resources used for serial input/output:

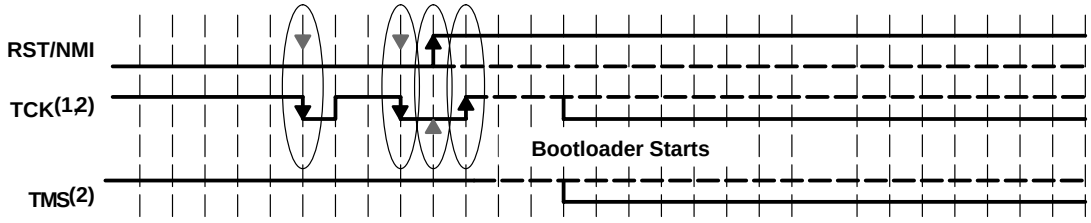
- Pins P1.1 and P2.2 for serial data transmission
- TCK and $\overline{\text{RST}}$/NMI to start program execution at the reset or bootstrap loader vector
- Basic clock module: Rsel=5, DCO=4, MOD=0, DCOCLK for MCLK and SMCLK, clock divider for MCLK and SMCLK at default: dividing by 1
- Timer_A: Timer_A operates in continuous mode with MCLK source selected, input divider set to 1, using CCR0, and polling of CCIFG0.
- WDT: Watchdog Timer is halted
- Interrupt: GIE=0, NMIIE=0, OFIE=0, ACCVIE=0
- Memory allocation and stack pointer:
  If the stack pointer points to RAM addresses above 0220h, 6 bytes of the stack are allocated, plus RAM addresses 0200h to 0219h. Otherwise the stack pointer is set to 0220h and allocates RAM from 0200h to 021Fh.

NOTE:
When writing RAM data via the bootstrap loader, make sure that the stack is outside the range of the data to be written.

Program execution begins with the user's reset vector at FFFEh (standard method) if TCK is held high while $\overline{\text{RST}}$/NMI goes from low to high:



Program execution begins with the bootstrap vector at 0C00h (boot ROM) if a minimum of two negative edges have been applied to TCK while $\overline{\text{RST}}$/NMI is low, and TCK is low when $\overline{\text{RST}}$/NMI goes from low to high.



boot ROM containing bootstrap loader (continued)

The bootstrap loader does not start (via the vector in address 0C00h) if:

- There are less than two negative edges at TCK while RST/NMI is low
- TCK is high when RST/NMI goes from low to high
- JTAG has control over the MSP430 resources
- The supply voltage VCC drops and a POR is executed

NOTES: 1. The default level of TCK is high. An active low has to be applied to enter the bootstrap loader. Other MSP430s which have a pin function used with a low default level can use an inverted signal.
2. The TMS signal must be high while TCK clocks are applied. This ensures that the JTAG controller function remains in its default mode.

WARNING:

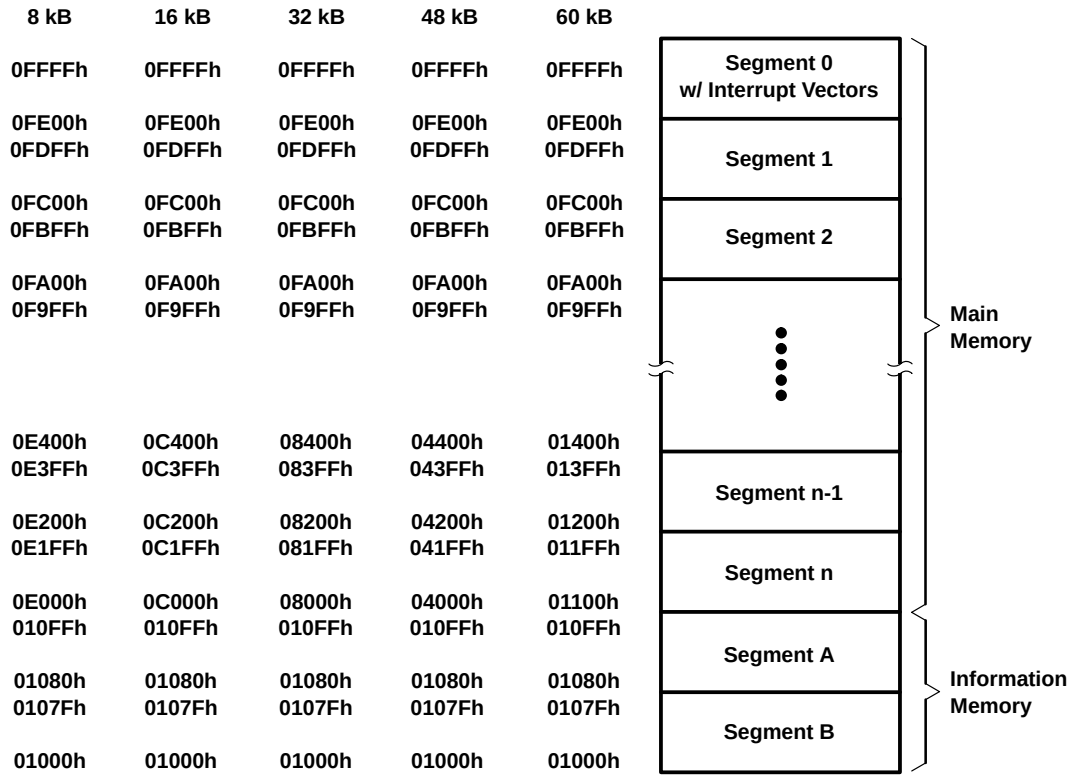
The bootstrap loader starts correctly only if the RST/NMI pin is in reset mode. Unpredictable program execution may result if it is switched to the NMI function. However, a bootstrap load may be started using software and the bootstrap vector, for example using the instruction BR &0C00h.

flash memory

MSP flash microcontrollers offer great flexibility because they can be reprogrammed. The flash memmory can be programmed through the JTAG port, through the bootstrap loader, or by the CPU itself. In addition, the CPU can perform single-byte and single-word writes to the flash memory. Other features of the flash memory include:

- Flash memory has n segments of main memory and two segments of information memory (A and B) of 128 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A and B can be erased individually, or as a group with segments 0–n.
  Segments A and B are also called *information memory.*
- A security fuse burning is irreversible; no further access to JTAG is possible afterwards
- Internal generation of the programming/erase voltage: no external V_{PP} has to be applied, but V_{CC} increases the supply current requirements.
- Program and erase timing is controlled by hardware in the flash memory—no software intervention is needed.
- The control hardware is called the flash-timing generator. The input frequency of the flash-timing generator should be in the proper range and should be maintained until the write/program or erase operation is completed.
- During program or erase, no code can be executed from flash memory and all interrupts must be disabled by setting the GIE, NMIIE, ACCVIE, and OFIE bits to zero. If a user program requires execution concurrent with a flash program or erase operation, the program must be executed from memory other than the flash memory (e.g., boot ROM, RAM). In the event a flash program or erase operation is initiated while the program counter is pointing to the flash memory, the CPU executes JMP $ instructions until the flash program or erase operation is completed. Normal execution of the previously running software then resumes.
- Unprogrammed, new devices may have some bytes programmed in the information memory (needed for test during manufacturing). The user should perform an erase of the information memory prior to first use.

flash memory (continued)



DMA controller

The MSP430x16x devices have a 3-channel DMA controller. The DMA controller is used to transfer data from one location to another without the CPU (see Figure 1). This allows for moving data from peripherals to RAM, RAM to peripherals, peripheral-to-peripheral, etc., completely without CPU intervention. The DMA controller enhances the ultralow-power capabilities of the MSP430 by allowing the CPU to remain in a low power mode while data transfers take place. In addition, the DMA capability enhances the processing power by speeding up data transfers, and can increase the throughput of the data converters as well.

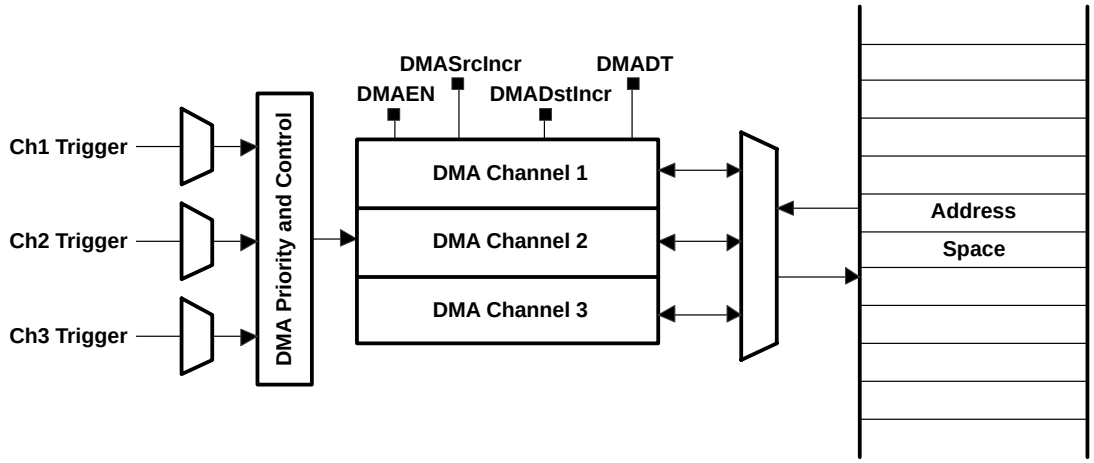


Figure 1. Block Diagram Direct Memory Access (DMA)

DMA controller (continued)

The MSP430x16x DMA controller supports four transfer modes. A fixed address can be transferred to a fixed address. A fixed address can be transferred to a block of addresses (e.g. transferring multiple A/D conversions to RAM). A block can be transferred to a fixed address (e.g. transferring multiple samples to a D/A converter). Or a block can be transferred to a block. In addition, the DMA controller supports the following features:

- Up to 3 DMA channels
- Configurable channel priorities
- Byte or word transfers
- Transfer blocks of any size
- Up to 16 sources to start the transfer(s)

peripherals

Peripherals are connected to the CPU through data, address, and control busses, and can be easily handled using all memory-manipulation instructions.

oscillator and system clock

Three clocks are used in the system—the main system (master) clock (MCLK) used by the CPU and the system, the subsystem (master) clock (SMCLK) used by the peripheral modules, and the auxiliary clock (ACLK) originated by LFXT1CLK (crystal frequency) and used by the peripheral modules.

Following a POR the DCOCLK is used by default, the DCOR bit is reset, and the DCO is set to the nominal initial frequency. Additionally, if either LFXT1CLK (with XT1 mode selected by XTS=1) or XT2CLK fails as the source for MCLK, DCOCLK is automatically selected to ensure fail-safe operation.

SMCLK can be generated from XT2CLK or DCOCLK. ACLK is always generated from LFXT1CLK.

Crystal oscillator LFXT1 can be defined to operate with watch crystals (32,768 Hz) or with higher-frequency ceramic resonators or crystals. The crystal or ceramic resonator is connected across two terminals. No external components are required for watch-crystal operation. If the high-frequency XT1 mode is selected, external capacitors from XIN to VSS and XOUT to VSS are required, as specified by the crystal manufacturer.

The LFXT1 oscillator starts after application of VCC. If the OscOff bit is set to 1, the oscillator stops when it is not used for MCLK.

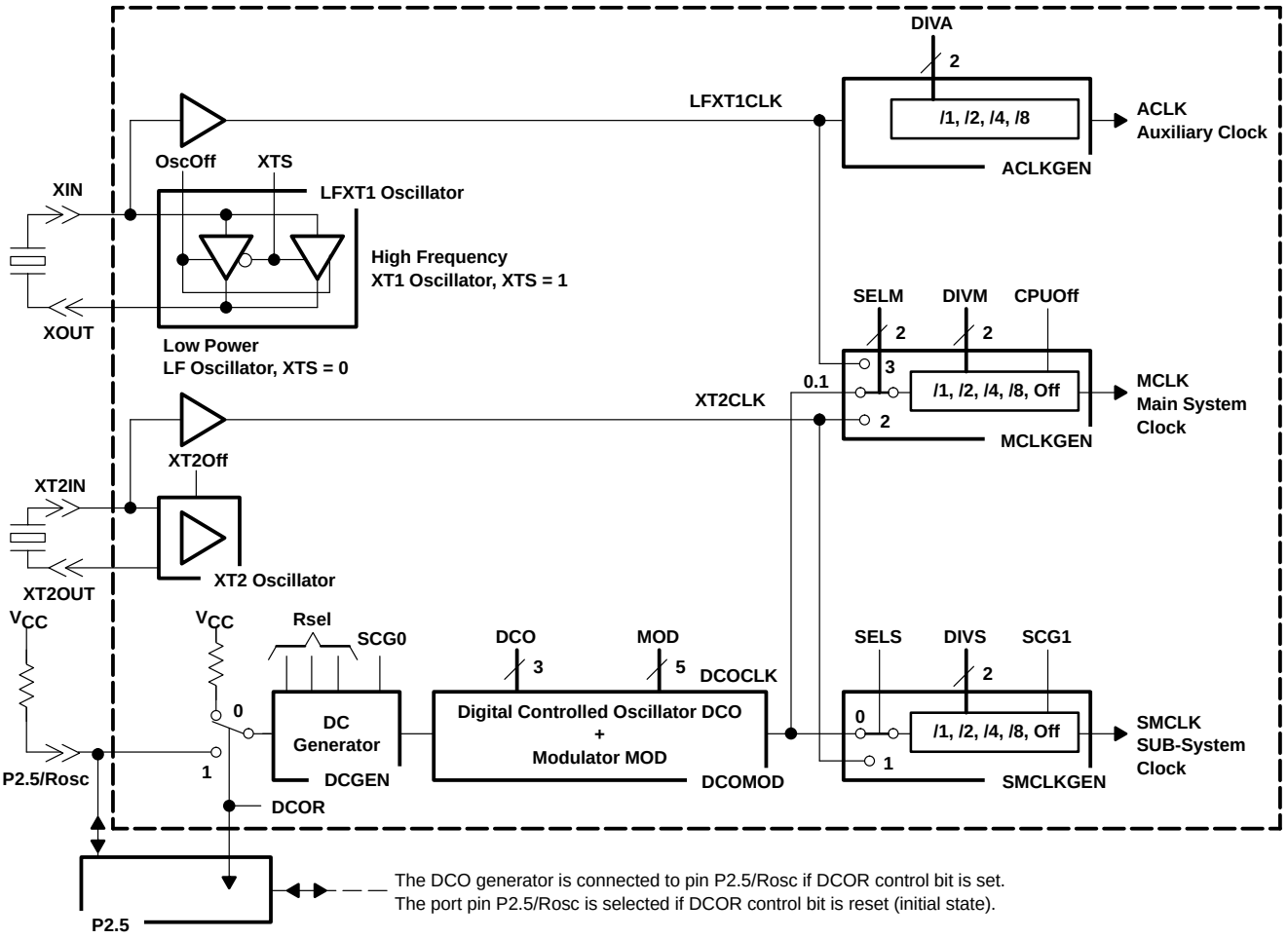
Crystal oscillator XT2 is identical to oscillator LFXT1, but only operates with higher-frequency ceramic resonators or crystals. The crystal or ceramic resonator is connected across two terminals. External capacitors from XT2IN to VSS and XT2OUT to VSS are required as specified by the crystal manufacturer.

The XT2 oscillator is off after application of VCC, since the XT2 oscillator control bit XT2Off is set. If bit XT2Off is set to 1, the XT2 oscillator stops when it is not used for MCLK or SMCLK.

Clock signals ACLK , MCLK, and SMCLK may be used externally via port pins.

Different application requirements and system conditions dictate different system-clock requirements, including:

- High frequency for quick reaction to system hardware requests or events
- Low frequency to minimize current consumption, EMI, etc.
- Stable peripheral clock for timer applications, such as real-time clock (RTC)
- Start-stop operation that can be enabled with minimum delay



brownout, supply voltage supervisor

The brownout circuit detects if a supply voltage is applied to or removed from the VCC terminal and resets the device appropriately. The CPU begins code execution after the brownout circuit releases the device reset. However, V_{CC} may not have ramped to $V_{CC(min)}$ at that time. The user must ensure the default FLL+ settings are not changed until V_{CC} reaches $V_{CC(min)}$. If desired, the SVS circuit can be used to determine when V_{CC} reaches $V_{CC(min)}$.

The supply voltage supervisor (SVS) circuitry detects if the supply voltage drops to a user selectable level and supports both supply voltage supervision (the device is automatically reset) and supply voltage monitoring (SVM, the device is not automatically reset). The SVS circuitry is shown in Figure 2. The initial condition for the SVS is off to conserve current consumption. The user's software should enable it when desired.

brownout, supply voltage supervisor (continued)

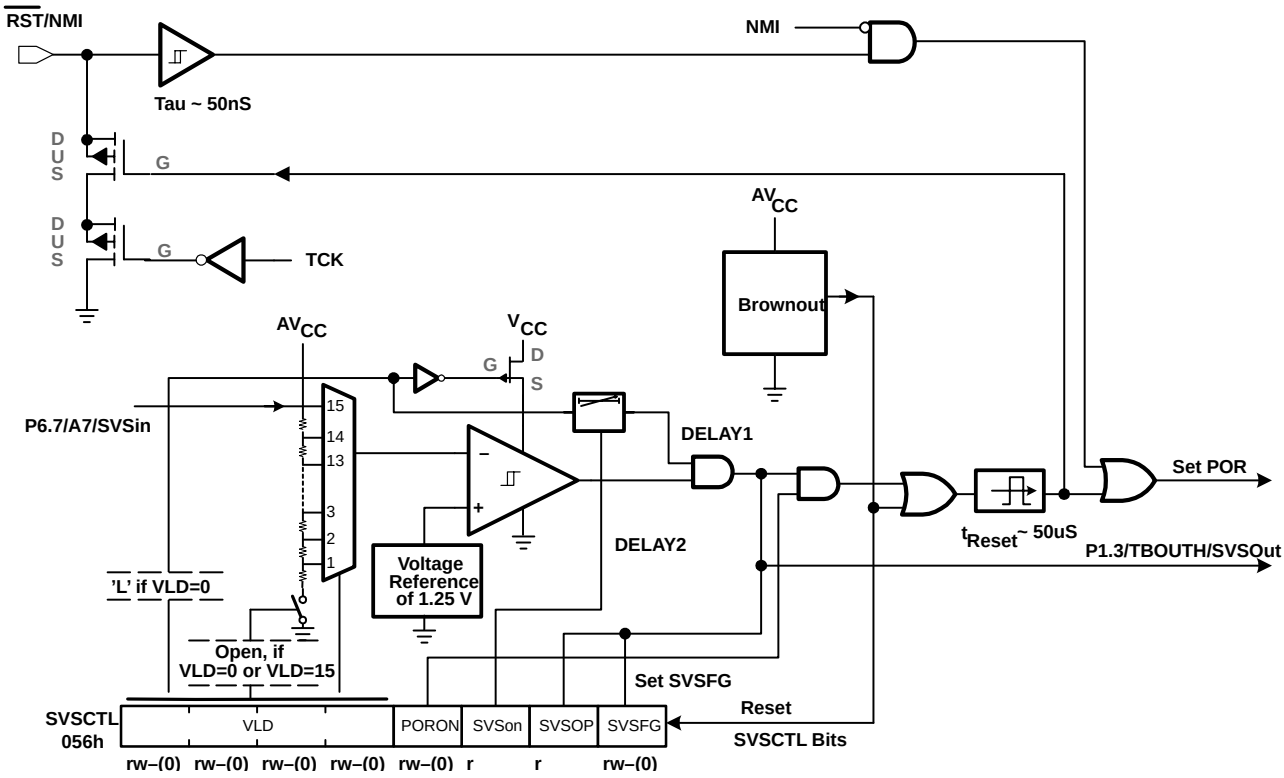


Figure 2. Block Diagram of Brownout and Supply Voltage Supervision

The VLD bits control the on/off state of the SVS circuitry. The SVS is off if VLD=0 and on if VLD=1. Bit PORON enables or disables the automatic reset of the MSP430 upon a low-voltage detection. If PORON=1, a low-voltage detection generates a POR signal and resets the MSP430. Bit SVSOP is used to watch the actual SVS comparator output. Bit SVSFG is set as long as a low-voltage situation is detected and remains set until no low voltage is detected and the software resets it. SVSFG latches such events, whereas SVSOP represents the actual output of the comparator.

If it is desired to only monitor the supply voltage, but not reset the device if it dips below the determined level, the user simply resets the PORON bit and sets the level normally. This provides the SVM function. The SVM function is useful for example, when performing A/D conversions and the user wants to know if the supply voltage dipped below the minimum operating voltage while the conversion took place.

The SVS circuitry uses hysteresis to reduce sensitivity on voltage drops when the VCC is close to the threshold level. The hysteresis for each SVS level is shown in the table below.

The SVS/SVM has some delay as shown below. The Delay1 (~50 µs) is used to avoid erroneous reset when the SVS/SVM is enabled (VLD changes from 0 to > 0). In addition, a second delay (DELAY2 = ~50 µs) holds the SVSon bit low whenever the value of VLD is changed. SVSon is low when VLD = 0.

The SVS level is user programmable as shown in the table below. In addition, any other voltage can be monitored if it is applied to A7.

brownout, supply voltage supervisor (continued)

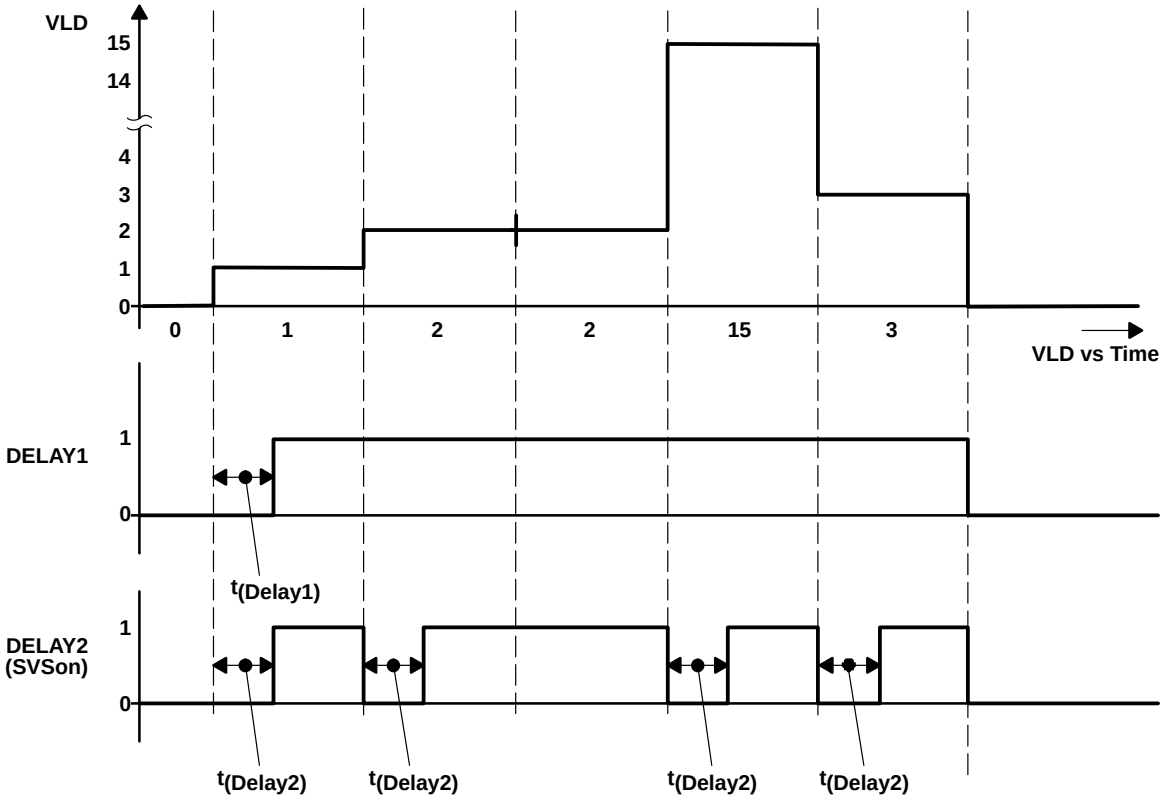


Figure 3. Timing of $t_{(Delay1)}$ and $t_{(Delay2)}$ Triggered by VLD

brownout, supply voltage supervisor (continued)

The levels for monitoring and supervision are defined by the control bits VLD:

VLD				$V_{CC(min)}$ [V]	COMMENT
0	0	0	0	NA	SVS/SVM function is off
0	0	0	1	1.9	SVS/SVM on. Hysteresis is typ 110 mV.
0	0	1	0	2.1	SVS/SVM on. Hysteresis is 8 mV to 30 mV.
0	0	1	1	2.2	SVS/SVM on. Hysteresis is 8 mV to 30 mV.
0	1	0	0	2.3	SVS/SVM on. Hysteresis is 8 mV to 30 mV.
0	1	0	1	2.4	SVS/SVM on. Hysteresis is 8 mV to 30 mV.
0	1	1	0	2.5	SVS/SVM on. Hysteresis is 8 mV to 30 mV.
0	1	1	1	2.65	SVS/SVM on. Hysteresis is 8 mV to 30 mV.
1	0	0	0	2.8	SVS/SVM on. Hysteresis is 8 mV to 30 mV.
1	0	0	1	2.9	SVS/SVM on. Hysteresis is 8 mV to 30 mV.
1	0	1	0	3.05	SVS/SVM on. Hysteresis is 8 mV to 30 mV.
1	0	1	1	3.2	SVS/SVM on. Hysteresis is 8 mV to 30 mV.
1	1	0	0	3.35	SVS/SVM on. Hysteresis is 8 mV to 30 mV.
1	1	0	1	3.5	SVS/SVM on. Hysteresis is 8 mV to 30 mV.
1	1	1	0	3.7†	SVS/SVM on. Hysteresis is 8 mV to 30 mV.
1	1	1	1	(1.2)	External analog input is used (input comes from the P6.7/A7/SVSin pin) and internally compared with 1.2 V.

† The recommended operation voltage range is limited to 3.6 V.

multiplication

The multiplication operation is supported by a dedicated peripheral module. The module performs 16 × 16, 16 × 8, 8 × 16, and 8 × 8 bit operations. The module is capable of supporting signed and unsigned multiplication as well as signed and unsigned multiply and accumulate operations. The result of an operation can be accessed immediately after the operands have been loaded into the peripheral registers. No additional clock cycles are required.

digital I/O

There are six 8-bit I/O ports implemented—ports P1 through P6. Ports P1 and P2 use seven control registers, while ports P3, P4, P5, and P6 use only four of the control registers to provide maximum digital input/output flexibility to the application:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Interrupt processing of external events is fully implemented for all eight bits of ports P1 and P2.
- Read/write access to all registers using all instructions is possible.

The seven control registers are:

- Input register — 8 bits at ports P1 through P6
- Output register — 8 bits at ports P1 through P6
- Direction register — 8 bits at ports P1 through P6
- Interrupt edge select — 8 bits at ports P1 and P2
- Interrupt flags — 8 bits at ports P1 and P2
- Interrupt enable — 8 bits at ports P1 and P2
- Selection (port or module) — 8 bits at ports P1 through P6

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digital I/O (continued)

Each one of these registers contains eight bits. Two interrupt vectors are implemented: one commonly used for any interrupt event on ports P1.0 to P1.7, and another commonly used for any interrupt event on ports P2.0 to P2.7.

Ports P3, P4, P5, and P6 have no interrupt capability.

Watchdog Timer

The primary function of the Watchdog Timer (WDT) module is to perform a controlled system restart after a software upset has occurred. A system reset is generated if the selected time interval expires. If an application does not require this watchdog function, the module can work as an interval timer, which generates an interrupt after a selected time interval.

The Watchdog Timer counter (WDTCNT) is a 15/16-bit up-counter not directly accessible by software. The WDTCNT is controlled using the Watchdog Timer control register (WDTCTL), which is an 8-bit read/write register. Writing to WDTCTL in either operating mode (watchdog or timer) is only possible when using the correct password (05Ah) in the high-byte. If any value other than 05Ah is written to the high-byte of the WDTCTL, a system reset PUC is generated. The password is read as 069h to minimize accidental write operations to the WDTCTL register. The low-byte stores data written to the WDTCTL. In addition to the Watchdog Timer control bits, there are two bits included in the WDTCTL that configure the NMI pin.

USART0

The universal serial interface module (USART0) is a dedicated peripheral module used in serial communications. The USART0 supports synchronous SPI (3-or 4-pin), asynchronous UART, and I^2C communication protocols using double-buffered transmit and receive channels. Data streams of 7 or 8 bits in length can be transferred at a rate determined by the program or by an external clock. Low-power applications are optimized by UART mode options which allow for the reception of only the first byte of a complete frame. The application software should then decide if the succeeding data is to be processed. This option reduces power consumption. Two dedicated interrupt vectors are assigned to the USART0 module, one for the receive and one for the transmit channel.

The I^2C support is compliant with the Phillips I^2C specification version 2.1 and supports standard mode (up to 100 kbps) and fast mode (up to 400 kbps). In addition, 7-bit and 10-bit device addressing modes are supported, as well as master and slave modes. The USART0 also supports 16-bit-wide I^2C data transfers and has two dedicated DMA channels to maximize bus throughput. Extensive interrupt capability is also given in the I^2C mode. NO TAG is the I^2C block diagram.

USART1

The universal synchronous/asynchronous interface is a dedicated peripheral module used in serial communications. The USART supports synchronous SPI (3- or 4-pin), and asynchronous UART communication protocols, using double-buffered transmit and receive channels. Data streams of 7 or 8 bits in length can be transferred at a rate determined by the program, or by an external clock. Low-power applications are optimized by UART mode options which allow for the reception of only the first byte of a complete frame. The application software should then decide if the succeeding data is to be processed. This option reduces power consumption.

Two dedicated interrupt vectors are assigned to each USART module—one for the receive and one for the transmit channels.

The function of USART1 is described in the applicable chapters of the *MSP430x1xx Family User's Guide*.

timer_A (three capture/compare registers)

The timer module offers one sixteen-bit counter and three capture/compare registers. The timer clock source can be selected from two external sources P1.0/TACLK (SSEL=0) or P2.1/TAINCLK (SSEL=3), or from two internal sources—ACLK (SSEL=1) or SMCLK (SSEL=2). The clock source can be divided by one, two, four, or eight. The timer can be fully controlled (in word mode)—it can be halted, read, and written; it can be stopped, run continuously, or made to count up or up/down using one compare block to determine the period. The three capture/compare blocks are configured by the application to run in capture or compare mode.

The capture mode is mostly used to individually measure internal or external events from any combination of positive, negative, or positive and negative edges. It can also be stopped by software. Three different external events can be selected: TA0, TA1, and TA2. In the capture/compare register CCR2, ACLK is the capture signal if CCI2B is selected. Software capture is chosen if CCISx=2 or CCISx=3.

The compare mode is mostly used to generate timing for the software or application hardware, or to generate pulse-width modulated output signals for various purposes like D/A conversion functions or motor control. An individual output module is assigned to each of the three capture/compare registers. This module can run independently of the compare function or can be triggered in several ways.

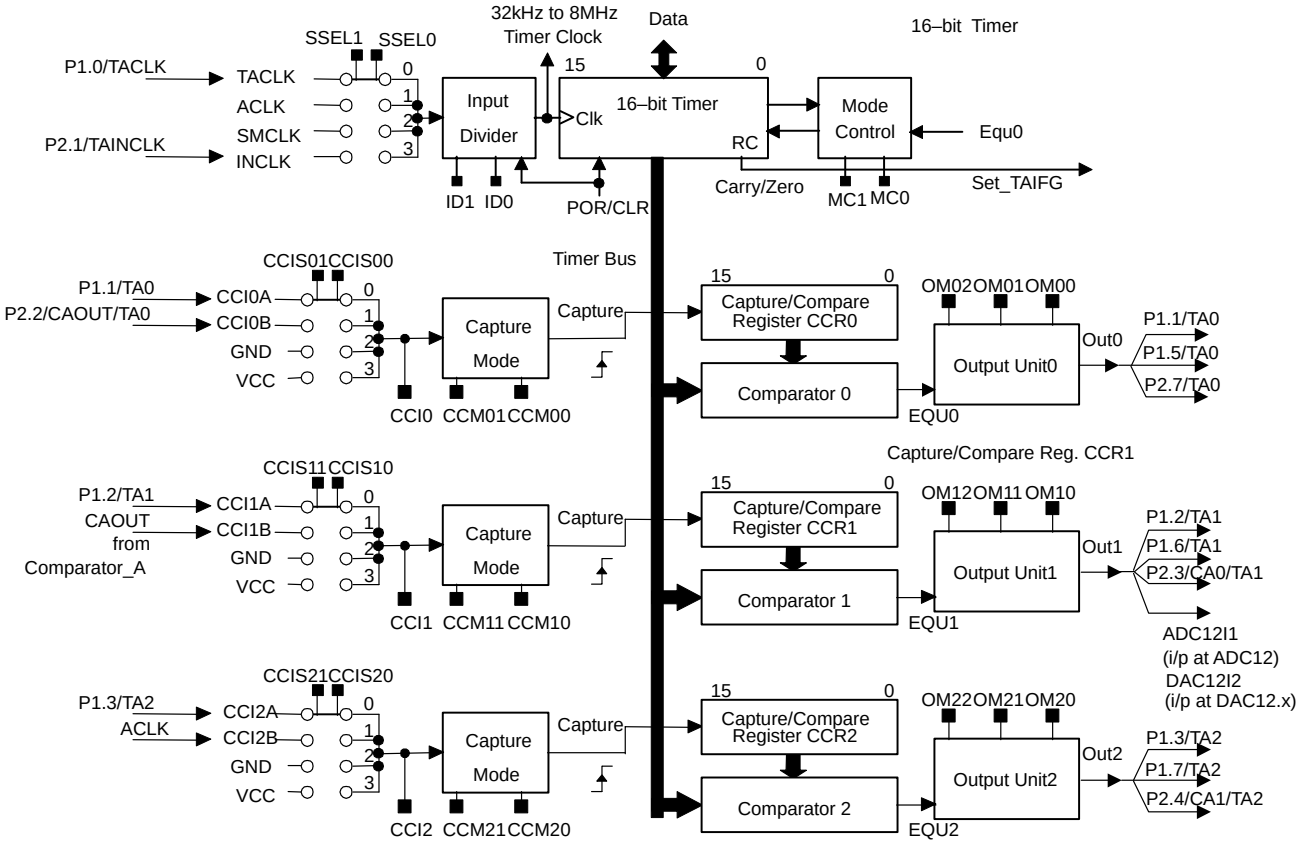

Figure 4. Timer_A, MSP430x15x/16x Configuration

Two interrupt vectors are used by the module. One vector is assigned to capture/compare block CCR0, and one common-interrupt vector is implemented for the timer and the other two capture/compare blocks. The three interrupt events using the same vector are identified by an individual interrupt vector word. The interrupt vector word is used to add an offset to the program counter so that the interrupt handler software continues at the corresponding program location. This simplifies the interrupt handler and assigns each interrupt event the same five-cycle overhead.

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timer_B (7 capture/compare registers in ’x16x and 3 capture/compare registers in ’x15x)

Timer_B7 is identical to Timer_A3, except for the following:

- The timer counter can be configured to operate in 8-, 10-, 12-, or 16-bit mode.
- The function of the capture/compare registers is slightly different when in compare mode. In Timer_B, the compare data is written to the capture/compare register, but is then transferred to the associated compare latch for the comparison.
- All output level Outx can be set to Hi-Z from the TboutH external signal.
- The SCCI bit is not implemented in Timer_B
- Timer_B7 has seven capture compare registers

The timer module has one sixteen-bit counter and seven capture/compare registers. The timer clock source can be selected from an external source TBCLK (SSEL=0 or 3), or from two internal sources: ACLK (SSEL=1) and SMCLK (SSEL=2)). The clock source can be divided by one, two, four, or eight. The timer can be fully controlled (in word mode): it can be halted, read, and written; it can be stopped, run continuously, or made to count up or up/down using one compare block to determine the period. The seven capture/compare blocks are configured by the application to run in capture or in compare mode.

The capture mode is mostly used to measure external or internal events from any combination of positive, negative, or positive and negative edges. It can also be stopped by software. Any of seven different external events TB0 to TB6 can be selected. In the capture/compare register CCR6, ACLK is the capture signal if CCI6B is selected. Software capture is chosen if CCISx=2 or CCISx=3.

The compare mode is mostly used to generate timing for the software or application hardware, or to generate pulse-width modulated output signals for various purposes such as D/A conversion functions or motor control. An individual output module is assigned to each of the seven capture/compare registers. This module can run independently of the compare function, or can be triggered in several ways. The comparison is made from the data in the compare latches (TBCLx) and not from the compare register.

Two interrupt vectors are used by the module. One vector is assigned to capture/compare block CCR0, and one common interrupt vector is implemented for the timer and the other six capture/compare blocks. The seven interrupt events using the same vector are identified by an individual interrupt vector word. The interrupt vector word is used to add an offset to the program counter so that the interrupt handler software continues at the corresponding program location. This simplifies the interrupt handler and assigns each interrupt event the same five-cycle overhead.

compare latches (TBCLx)

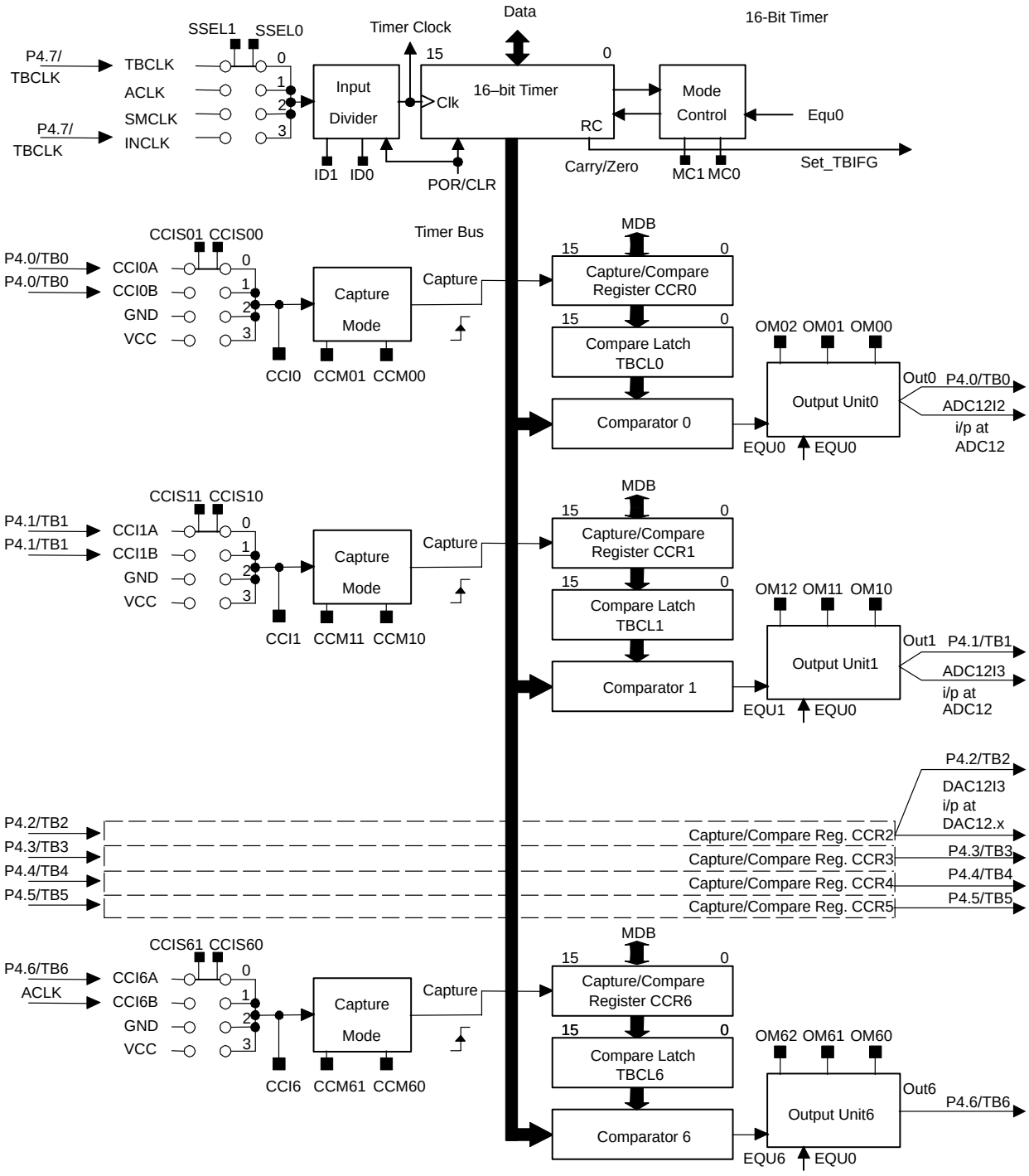
The compare latches can be loaded directly by software or via selected conditions triggered by the PWM function. They are reset by the POR signal.

Load TBCLx immediate, CLLD=0:	Capture/compare register CCRx and the corresponding compare latch are loaded simultaneously.
Load TBCLx at Zero, CLLD=1:	The data in capture/compare register CCRx is loaded to the corresponding compare latch when the 16-bit timer TBR counts to zero.
Load TBCLx at Zero + Period, CLLD=2:	The data in capture/compare register CCRx is loaded to the corresponding compare latch when the 16-bit timer TBR counts to zero or when the next period starts (in UP/DOWN mode).
Load TBCLx at EQUx, CLLD=3:	The data in capture/compare register CCRx is loaded when CCRx is equal to TBR.

Loading the compare latches can be done individually or in groups. Individually means that whenever the selected load condition (see above) is true, the CCRx data is loaded into TBCLx.

Load TBCLx individually, TBCLGRP=0:	Compare latch TBCLx is loaded when the selected load condition (CLLD) is true.
Dual load TBCLx mode, TBCLGRP=1:	Two compare latches TBCLx are loaded when data are written to both CCRx registers of the same group and the load condition (CLLD) is true. Three groups are defined: CCR1+CCR2, CCR3+CCR4, and CCR5+CCR6.
Triple load TBCLx mode, TBCLGRP=2:	Three compare latches TBCLx are loaded when data are written to all CCRx registers of the same group and then the selected load condition (CLLD) is true. Two groups are defined: CCR1+CCR2+CCR3 and CR4+CCR5+CCR6.
Full load TBCLx mode, TBCLGRP=3:	All seven compare latches TBCLx are loaded when data are written to all seven CCRx registers and then the selected load condition (CLLD) is true. All CCRx data, CCR0+CCR1+CCR2+CCR3+CCR4+CCR5+CCR6, are simultaneously loaded to the corresponding SHRx compare latches.

compare latches (TBCLx) (continued)



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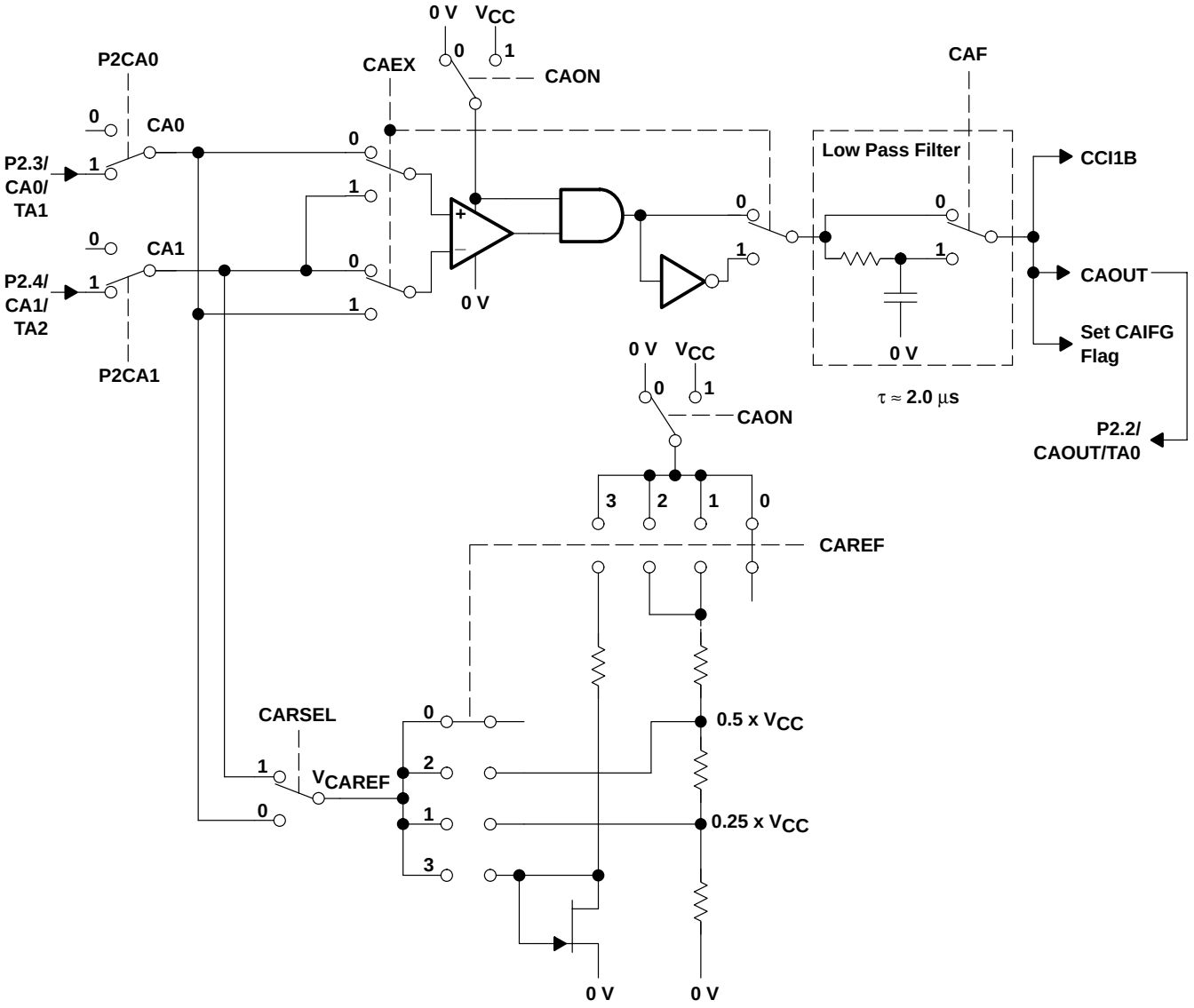
comparator_A

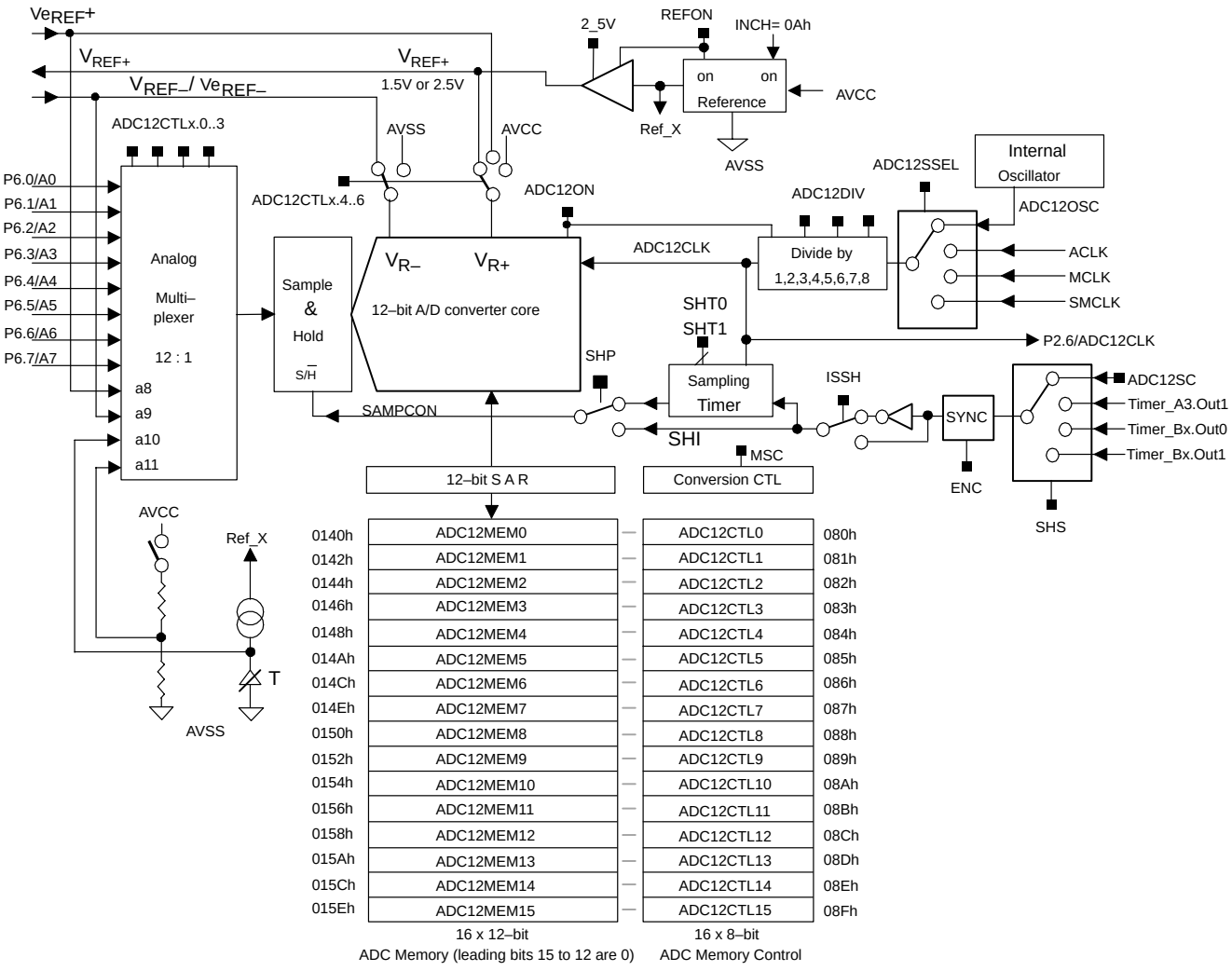
The primary functions of the comparator module are support of precision slope conversion in A/D applications, battery voltage supervision, and external analog signal monitoring. The comparator is connected to port pins P2.3 (+ terminal) and to P2.4 (–terminal). It is controlled via eight control bits in the CACTL register.



A/D converter

The 12-bit analog-to-digital converter (ADC) uses a 10-bit weighted capacitor array plus a 2-bit resistor string. The CMOS threshold detector in the successive-approximation conversion technique determines each bit by examining the charge on a series of binary-weighted capacitors. The features of the ADC are:

- 12-bit converter with ±1 LSB linearity
- Built-in sample-and-hold
- Eight external and four internal analog channels. The external ADC input terminals are shared with digital port I/O pins.
- Internal reference voltage V_{REF+} of 1.5 V or 2.5 V, software-selectable by control bit 2_5V
- Internal-temperature sensor for temperature measurement
  T = (V_SENSOR(T) – V_SENSOR(0°C)) / TC_SENSOR in °C
- Battery-voltage measurement: $N = 0.5 \times (AV_{CC} - AV_{SS}) \times 4096/1.5V$; $V_{REF}+$ is selected for 1.5 V.
- Source of positive reference voltage level V_{R+} can be selected as internal (1.5 V or 2.5 V), external, or AV_{CC}. The source is selected individually for each channel.
- Source of negative reference voltage level V_{R-} can be selected as external or AV_{SS}. The source is selected individually for each channel.
- Conversion time can be selected from various clock sources: ACLK, MCLK, SMCLK, or the internal ADC12CLK oscillator. The clock source is divided by an integer from 1 to 8, as selected by software.
- Channel conversion: individual channels, a group of channels, or repeated conversion of a group of channels. If conversion of a group of channels is selected, the sequence, the channels, and the number of channels in the group can be defined by software. For example, a1-a2-a5-a2-a2-….
- The conversion is enabled by the ENC bit, and can be triggered by software via sample and conversion control bit ADC12SC, Timer_A3, or Timer_Bx. Most of the control bits can be modified only if ENC control bit is low. This prevents unpredictable results caused by unintended modification.
- Sampling time can be $4 \times n0 \times$ ADC12CLK or $4 \times n1 \times$ ADC12CLK. It can be selected to sample as long as the sample signal is high (ISSH=0) or low (ISSH=1). SHT0 defines n0 and SHT1 defines n1.
- The conversion result is stored in one of sixteen registers. The sixteen registers have individual addresses and can be accessed via software. Each of the sixteen registers is linked to an 8-bit register that defines the positive and negative reference source and the channel assigned.



DAC12

The MP430F15x and MP430F16x devices have dual 12-bit DACs. Each DAC12 module is a 12-bit R-ladder, voltage-output DAC. Each DAC12 module can use AV_{CC} for the positive reference (applied at $V_{e(REF+)}$), or can use either the 1.5-V or the 2.5-V reference signal from the ADC12 module.

Each DAC12 module is highly configurable. The update of each DAC can be individually selectable to occur on an output event from Timer_A or Timer_B, or can occur immediately after data is written to the respective DAC12xDAT register. In addition, the DAC12 modules can be synchronized such that they update simultaneously.

Applications may benefit from using the DAC12 modules together with the DMA channels. With the DMA capability, the user can store DAC values in memory and have them automatically transferred to each DAC12 module. This allows the capability to create two independent, periodic waveforms, conpletely controlled by hardware, without any CPU intervention. The DAC12 block diagram is shown in Figure 5.

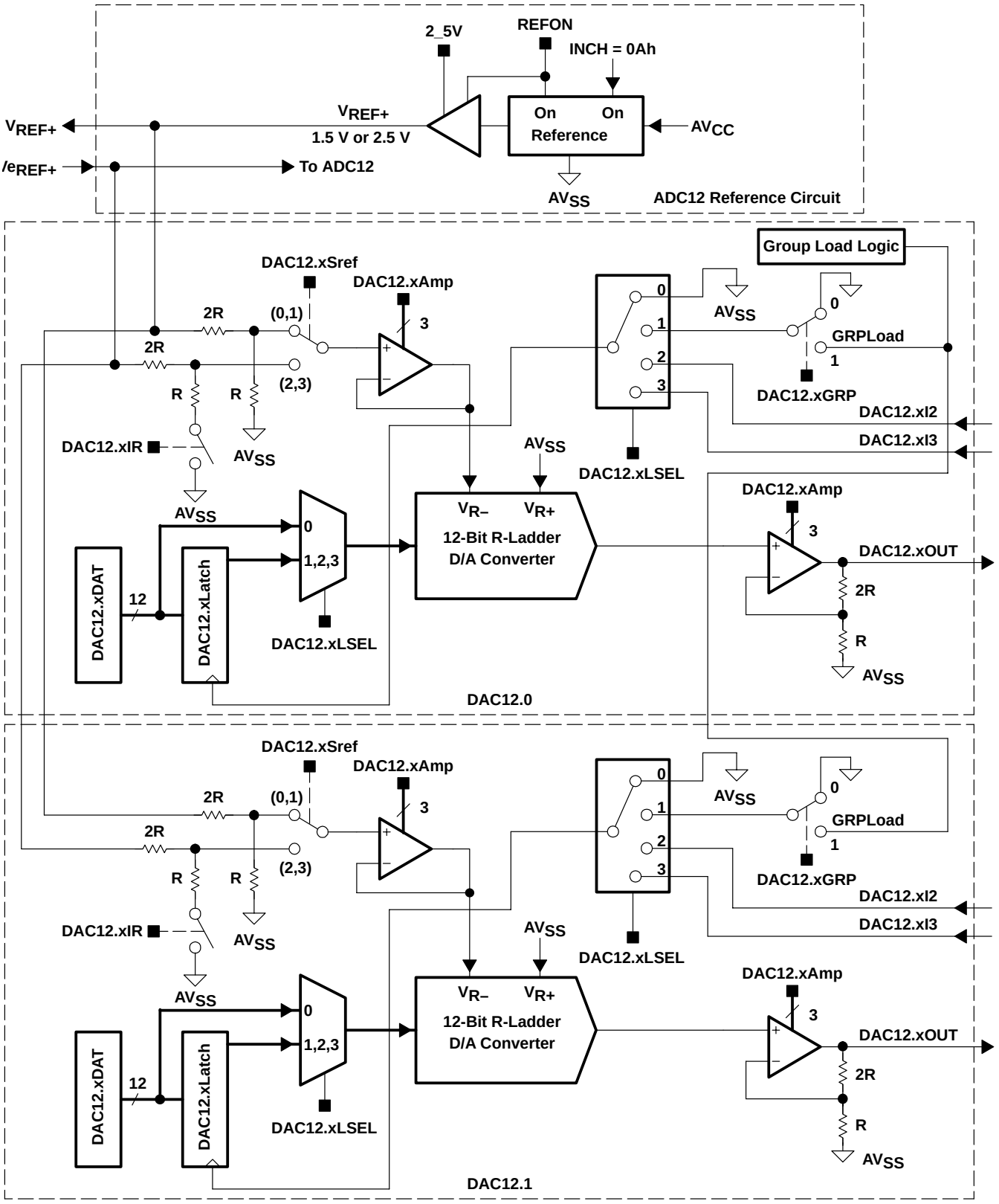


Figure 5. DAC12 Block Diagram

peripheral file map

PERIPHERAL FILE MAP			
DMA	DMA channel 2 transfer size	DMA2Sz	01F6h
	DMA channel 2 destination address	DMA2DA	01F4h
	DMA channel 2 source address	DMA2SA	01F2h
	DMA channel 1 transfer size	DMA1Sz	01EEh
	DMA channel 1 destination address	DMA1DA	01ECh
	DMA channell 1 source address	DMA0SA	01EAh
	DMA channel 0 transfer size	DMA0Sz	01E6h
	DMA channel 0 destination address	DMA0DA	01E4h
	DMA channel 0 source address	DMA0SA	01E2h
	DMA channel 2 control	DMA2CTL	01F0h
	DMA channel 1 control	DMA1CTL	01E8h
	DMA channel 0 control	DMA0CTL	01E0h
	DMA module control 1	DMACTL1	0124h
	DMA module control 0	DMACTL0	0122h
DAC12	DAC12.1 data	DAC12_1DAT	01CAh
	DAC12.1 control	DAC12_1CTL	01C2h
	DAC12.0 data	DAC12_0DAT	01C8h
	DAC12.0 control	DAC12_0CTL	01C0h
ADC12	Interrupt-vector-word register	ADC12IV	01A8h
	Inerrupt-enable register	ADC12IE	01A6h
	Inerrupt-flag register	ADC12IFG	01A4h
	Control register 1	ADC12CTL1	01A2h
	Control register 0	ADC12CTL0	01A0h
	Conversion memory 15	ADC12MEM15	015Eh
	Conversion memory 14	ADC12MEM14	015Ch
	Conversion memory 13	ADC12MEM13	015Ah
	Conversion memory 12	ADC12MEM12	0158h
	Conversion memory 11	ADC12MEM11	0156h
	Conversion memory 10	ADC12MEM10	0154h
	Conversion memory 9	ADC12MEM9	0152h
	Conversion memory 8	ADC12MEM8	0150h
	Conversion memory 7	ADC12MEM7	014Eh
	Conversion memory 6	ADC12MEM6	014Ch
	Conversion memory 5	ADC12MEM5	014Ah
	Conversion memory 4	ADC12MEM4	0148h
	Conversion memory 3	ADC12MEM3	0146h
	Conversion memory 2	ADC12MEM2	0144h
	Conversion memory 1	ADC12MEM1	0142h
	Conversion memory 0	ADC12MEM0	0140h

peripheral file map (continued)

PERIPHERAL FILE MAP (CONTINUED)			
ADC12 (continued)	ADC memory-control register15	ADC12MCTL15	08Fh
	ADC memory-control register14	ADC12MCTL14	08Eh
	ADC memory-control register13	ADC12MCTL13	08Dh
	ADC memory-control register12	ADC12MCTL12	08Ch
	ADC memory-control register11	ADC12MCTL11	08Bh
	ADC memory-control register10	ADC12MCTL10	08Ah
	ADC memory-control register9	ADC12MCTL9	089h
	ADC memory-control register8	ADC12MCTL8	088h
	ADC memory-control register7	ADC12MCTL7	087h
	ADC memory-control register6	ADC12MCTL6	086h
	ADC memory-control register5	ADC12MCTL5	085h
	ADC memory-control register4	ADC12MCTL4	084h
	ADC memory-control register3	ADC12MCTL3	083h
	ADC memory-control register2	ADC12MCTL2	082h
	ADC memory-control register1	ADC12MCTL1	081h
	ADC memory-control register0	ADC12MCTL0	080h
Timer_B7/ Timer_B3 (see Note 1)	Capture/compare register 6	CCR6	019Eh
	Capture/compare register 5	CCR5	019Ch
	Capture/compare register 4	CCR4	019Ah
	Capture/compare register 3	CCR3	0198h
	Capture/compare register 2	CCR2	0196h
	Capture/compare register 1	CCR1	0194h
	Capture/compare register 0	CCR0	0192h
	Timer_B register	TBR	0190h
	Capture/compare control 6	CCTL6	018Eh
	Capture/compare control 5	CCTL5	018Ch
	Capture/compare control 4	CCTL4	018Ah
	Capture/compare control 3	CCTL3	0188h
	Capture/compare control 2	CCTL2	0186h
	Capture/compare control 1	CCTL1	0184h
	Capture/compare control 0	CCTL0	0182h
	Timer_B control	TBCTL	0180h
	Timer_B interrupt vector	TBIV	011Eh
Timer_A3	Reserved		017Eh
	Reserved		017Ch
	Reserved		017Ah
	Reserved		0178h
	Capture/compare register 2	CCR2	0176h
	Capture/compare register 1	CCR1	0174h
	Capture/compare register 0	CCR0	0172h
	Timer_A register	TAR	0170h
	Reserved		016Eh
	Reserved		016Ch
	Reserved		016Ah
	Reserved		0168h

NOTE 1: Timer_B7 in MSP430x16x family has 7 CCR, Timer_B3 in MSP430x15x family has 3 CCR.

peripheral file map (continued)

PERIPHERAL FILE MAP (CONTINUED)			
Timer_A3 (continued)	Capture/compare control 2	CCTL2	0166h
	Capture/compare control 1	CCTL1	0164h
	Capture/compare control 0	CCTL0	0162h
	Timer_A control	TACTL	0160h
	Timer_A interrupt vector	TAIV	012Eh
Multiplier (MSP430x16x only)	Sum extend	SumExt	013Eh
	Result high word	ResHi	013Ch
	Result low word	ResLo	013Ah
	Second operand	OP_2	0138h
	Multiply signed +accumulate/operand1	MACS	0136h
	Multiply+accumulate/operand1	MAC	0134h
	Multiply signed/operand1	MPYS	0132h
	Multiply unsigned/operand1	MPY	0130h
Flash	Flash control 3	FCTL3	012Ch
	Flash control 2	FCTL2	012Ah
	Flash control 1	FCTL1	0128h
Watchdog	Watchdog Timer control	WDTCTL	0120h
USART1 (Only in ’x16x)	Transmit buffer	UTXBUF1	07Fh
	Receive buffer	URXBUF1	07Eh
	Baud rate	UBR11	07Dh
	Baud rate	UBR01	07Ch
	Modulation control	UMCTL1	07Bh
	Receive control	URCTL1	07Ah
	Transmit control	UTCTL1	079h
	USART control	UCTL1	078h
USART0 (UART or SPI mode)	Transmit buffer	UTXBUF0	077h
	Receive buffer	URXBUF0	076h
	Baud rate	UBR10	075h
	Baud rate	UBR00	074h
	Modulation control	UMCTL0	073h
	Receive control	URCTL0	072h
	Transmit control	UTCTL0	071h
	USART control	UCTL0	070h
USART0 (I^2C mode)	I2C interrupt vector	I2CIV	011Ch
	I2C slave address	I2CSA	011Ah
	I2C own address	I2COA	0118h
	I2C data	I2CDR	076h
	I2C SCLL	I2CSCLL	075h
	I2C SCLH	I2CSCLH	074h
	I2C PSC	I2CPSC	073h
	I2C data control	I2CDCTL	072h
	I2C transfer control	I2CTCTL	071h
	USART control	UCTL0	070h
	I2C data count	I2CNDAT	052h
	I2C interrupt flag	I2CIFG	051h
	I2C interrupt enable	I2CIE	050h

peripheral file map (continued)

PERIPHERAL FILE MAP (CONTINUED)			
Comparator_A	Comp._A port disable	CAPD	05Bh
	Comp._A control2	CACTL2	05Ah
	Comp._A control1	CACTL1	059h
System Clock	Basic clock system control2	BCSCTL2	058h
	Basic clock system control1	BCSCTL1	057h
	DCO clock frequency control	DCOCTL	056h
Port P6	Port P6 selection	P6SEL	037h
	Port P6 direction	P6DIR	036h
	Port P6 output	P6OUT	035h
	Port P6 input	P6IN	034h
Port P5	Port P5 selection	P5SEL	033h
	Port P5 direction	P5DIR	032h
	Port P5 output	P5OUT	031h
	Port P5 input	P5IN	030h
Port P4	Port P4 selection	P4SEL	01Fh
	Port P4 direction	P4DIR	01Eh
	Port P4 output	P4OUT	01Dh
	Port P4 input	P4IN	01Ch
Port P3	Port P3 selection	P3SEL	01Bh
	Port P3 direction	P3DIR	01Ah
	Port P3 output	P3OUT	019h
	Port P3 input	P3IN	018h
Port P2	Port P2 selection	P2SEL	02Eh
	Port P2 interrupt enable	P2IE	02Dh
	Port P2 interrupt-edge select	P2IES	02Ch
	Port P2 interrupt flag	P2IFG	02Bh
	Port P2 direction	P2DIR	02Ah
	Port P2 output	P2OUT	029h
	Port P2 input	P2IN	028h
Port P1	Port P1 selection	P1SEL	026h
	Port P1 interrupt enable	P1IE	025h
	Port P1 interrupt-edge select	P1IES	024h
	Port P1 interrupt flag	P1IFG	023h
	Port P1 direction	P1DIR	022h
	Port P1 output	P1OUT	021h
	Port P1 input	P1IN	020h
Special Functions	SFR module enable 2	ME2	005h
	SFR module enable 1	ME1	004h
	SFR interrupt flag2	IFG2	003h
	SFR interrupt flag1	IFG1	002h
	SFR interrupt enable2	IE2	001h
	SFR interrupt enable1	IE1	000h

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Voltage applied at V_{CC} to V_{SS} . . . . . –0.3 V to + 4.1 V
Voltage applied to any pin (referenced to V_{SS}) . . . . . –0.3 V to V_{CC}+0.3 V
Diode current at any device terminal . . . . . ±2 mA
Storage temperature (unprogrammed device) . . . . . –55°C to 150°C
Storage temperature (programmed device) . . . . . –40°C to 85°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE: All voltages referenced to V_{SS}.

recommended operating conditions

PARAMETER			MIN	NOM	MAX	UNITS
Supply voltage during program execution, V_{CC} (AV_{CC} = DV_{CC} = V_{CC})		MSP430F15x, MSP430F16x	1.8		3.6	V
Supply voltage during flash memory programming, V_{CC} (AV_{CC} = DV_{CC} = V_{CC})		MSP430F15x, MSP430F16x	2.7		3.6	V
Supply voltage, V_{SS}			0.0		0.0	V
Operating free-air temperature range, T_A		MSP430x15x MSP430x16x	–40		85	°C
LFXT1 crystal frequency, $f_{(LFXT1)}$ (see Notes 1 and 2)	LF selected, XTS=0	Watch crystal		32768		Hz
	XT1 selected, XTS=1	Ceramic resonator	450		8000	kHz
	XT1 selected, XTS=1	Crystal	1000		8000	kHz
XT2 crystal frequency, $f_{(XT2)}$		Ceramic resonator	450		8000	kHz
		Crystal	1000		8000	
Processor frequency (signal MCLK), $f_{(System)}$		V_{CC} = 1.8 V	DC		4.15	MHz
		V_{CC} = 3.6 V	DC		8	
Flash-timing-generator frequency, $f_{(FTG)}$		MSP430F15x, MSP430F16x	257		476	kHz
Cumulative program time, $t_{(CPT)}$ (see Note 3)		V_{CC} = 2.7 V/3.6 V MSP430F15x MSP430F16x			3	ms
Mass erase time, t(MEras) (See also the *flash memory, timing generator, control register FCTL2* section, see Note 4)		V_{CC} = 2.7 V/3.6 V	200			ms
Low-level input voltage (TCK, TMS, TDI, RST/NMI), V_{IL} (excluding Xin, Xout)		V_{CC} = 2.2 V/3 V	V_{SS}		V_{SS} +0.6	V
High-level input voltage (TCK, TMS, TDI, RST/NMI), V_{IH} (excluding Xin, Xout)		V_{CC} = 2.2 V/3 V	0.8V_{CC}		V_{CC}	V
Input levels at Xin and Xout	$V_{IL(Xin, Xout)}$	V_{CC} = 2.2 V/3 V	V_{SS}		0.2×V_{SS}	V
	$V_{IH(Xin, Xout)}$		0.8×V_{CC}		V_{CC}	

NOTES: 1. In LF mode, the LFXT1 oscillator requires a watch crystal and the LFXT1 oscillator requires a 5.1-MΩ resistor from XOUT to VSS when VCC < 2.5 V. In XT1 mode, the LFXT1 and XT2 oscillators accept a ceramic resonator or a 4-MHz crystal frequency at $V_{CC} \geq$ 2.2 V. In XT1 mode, the LFXT1 and XT2 oscillators accept a ceramic resonator or an 8-MHz crystal frequency at $V_{CC} \geq$ 2.8 V.
2. In LF mode, the LFXT1 oscillator requires a watch crystal. In XT1 mode, FXT1 accepts a ceramic resonator or a crystal.
3. The cumulative program time must not be exceeded during a block-write operation. This parameter is only relevant if segment write option is used.
4. The mass erase duration generated by the flash timing generator is at least 11.1 ms. The cummulative mass erase time needed is 200 ms. This can be achieved by repeating the mass erase operation until the cumulative mass erase time is met (a minimum of 19 cycles may be required).

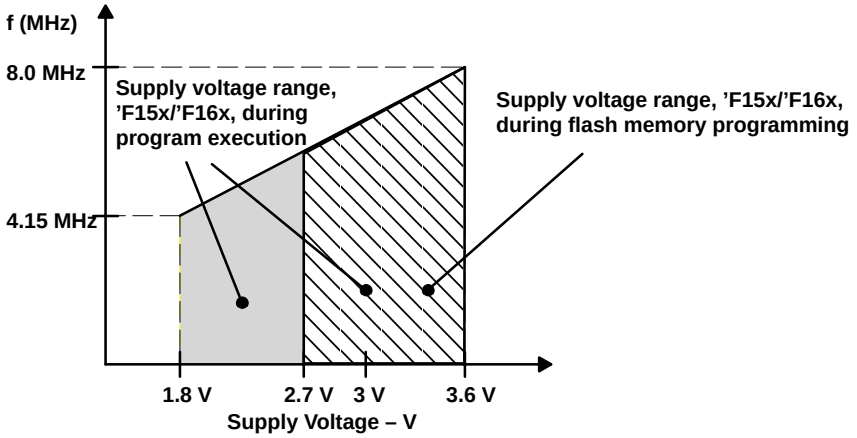


Figure 6. Frequency vs Supply Voltage, MSP430F15x or MSP430F16x

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

supply current into AV_{CC} + DV_{CC} excluding external current, $f_{(System)}$ = 1 MHz

PARAMETER			TEST CONDITIONS		MIN	NOM	MAX	UNIT
$I_{(AM)}$	Active mode, (see Note 1) $f_{(MCLK)} = f_{(SMCLK)}$ = 1 MHz, $f_{(ACLK)}$ = 32,768 Hz XTS=0, SELM=(0,1)	F15x, F16x	T_A = –40°C to 85°C	V_{CC} = 2.2 V		280	350	µA
				V_{CC} = 3 V		420	560	
$I_{(LPM0)}$	Low-power mode, (LPM0) (see Note 1)	F15x, F16x	T_A = –40°C to 85°C	V_{CC} = 2.2 V		32	45	µA
				V_{CC} = 3 V		55	70	
$I_{(LPM2)}$	Low-power mode, (LPM2), f(MCLK) = f (SMCLK) = 0 MHz, f(ACLK) = 32.768 Hz, SCG0 = 0		T_A = –40°C to 85°C	V_{CC} = 2.2 V		11	14	µA
				V_{CC} = 3 V		17	22	
$I_{(LPM3)}$	Low-power mode, (LPM3) $f_{(MCLK)} = f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 32,768 Hz, SCG0 = 1 (see Note 2)		T_A = –40°C	V_{CC} = 2.2 V		0.8	1.5	µA
			T_A = 25°C			0.9	1.5	
			T_A = 85°C			1.6	2.8	
			T_A = –40°C	V_{CC} = 3 V		1.8	2.2	µA
			T_A = 25°C			1.6	1.9	
			T_A = 85°C			2.3	3.9	
$I_{(LPM4)}$	Low-power mode, (LPM4) $f_{(MCLK)}$ = 0 MHz, $f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 0 Hz, SCG0 = 1		T_A = –40°C	V_{CC} = 2.2 V		0.1	0.5	µA
			T_A = 25°C			0.1	0.5	
			T_A = 85°C			0.8	2.5	
			T_A = –40°C	V_{CC} = 3 V		0.1	0.5	µA
			T_A = 25°C			0.1	0.5	
			T_A = 85°C			0.8	2.5	

NOTES: 1. Timer_B is clocked by f(DCOCLK) = 1 MHz. All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
2. Timer_B is clocked by f(ACLK) = 32,768 Hz. All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current. The current consumption in LPM2 and LPM3 are measured with ACLK selected.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

Current consumption of active mode versus system frequency, F-version

$I(AM) = I(AM)\ [1\ MHz] \times f(System)\ [MHz]$

Current consumption of active mode versus supply voltage, F-version

$I_{(AM)} = I_{(AM)\ [3\ V]} + 175\ \mu A/V \times (V_{CC} - 3\ V)$

SCHMITT-trigger inputs – Ports P1, P2, P3, P4, P5, and P6

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 2.2 V	1.1		1.5	V
		V_{CC} = 3 V	1.5		1.9	
V_{IT-}	Negative-going input threshold voltage	V_{CC} = 2.2 V	0.4		0.9	V
		V_{CC} = 3 V	0.90		1.3	
V_{hys}	Input voltage hysteresis ($V_{IT+} - V_{IT-}$)	V_{CC} = 2.2 V	0.3		1.1	V
		V_{CC} = 3 V	0.5		1	

standard inputs – RST/NMI; JTAG: TCK, TMS, TDI, TDO/TDI

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage	V_{CC} = 2.2 V / 3 V	V_{SS}		V_{SS}+0.6	V
V_{IH}	High-level input voltage		0.8×V_{CC}		V_{CC}	V

outputs – Ports P1, P2, P3, P4, P5, and P6

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH(max)}$ = –1 mA,	V_{CC} = 2.2 V,	See Note 1	V_{CC}–0.25		V_{CC}	V
		$I_{OH(max)}$ = –3.4 mA,	V_{CC} = 2.2 V,	See Note 2	V_{CC}–0.6		V_{CC}	
		$I_{OH(max)}$ = –1 mA,	V_{CC} = 3 V,	See Note 1	V_{CC}–0.25		V_{CC}	
		$I_{OH(max)}$ = –3.4 mA,	V_{CC} = 3 V,	See Note 2	V_{CC}–0.6		V_{CC}	
V_{OL}	Low-level output voltage	$I_{OL(max)}$ = 1.5 mA,	V_{CC} = 2.2 V,	See Note 1	V_{SS}		V_{SS}+0.25	V
		$I_{OL(max)}$ = 6 mA,	V_{CC} = 2.2 V,	See Note 2	V_{SS}		V_{SS}+0.6	
		$I_{OL(max)}$ = 1.5 mA,	V_{CC} = 3 V,	See Note 1	V_{SS}		V_{SS}+0.25	
		$I_{OL(max)}$ = 6 mA,	V_{CC} = 3 V,	See Note 2	V_{SS}		V_{SS}+0.6	

NOTES: 1. The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±6 mA to satisfy the maximum specified voltage drop.
2. The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±24 mA to satisfy the maximum specified voltage drop.

outputs – Ports P1, P2, P3, P4, P5, and P6 (continued)

TYPICAL LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE

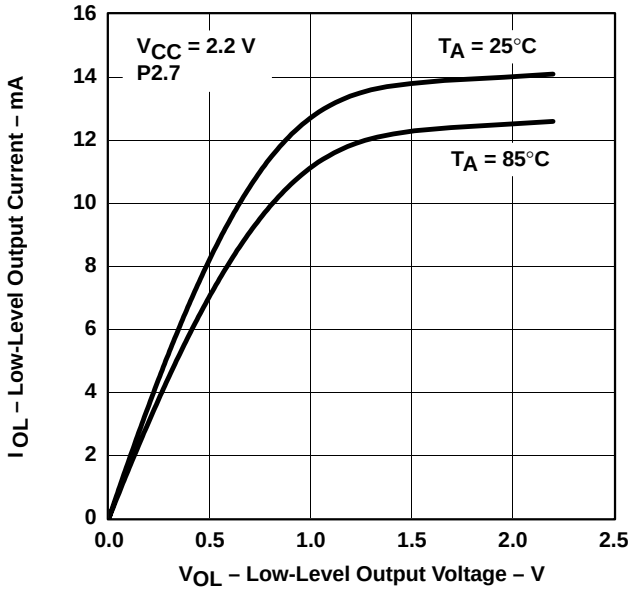


Figure 7

TYPICAL LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE

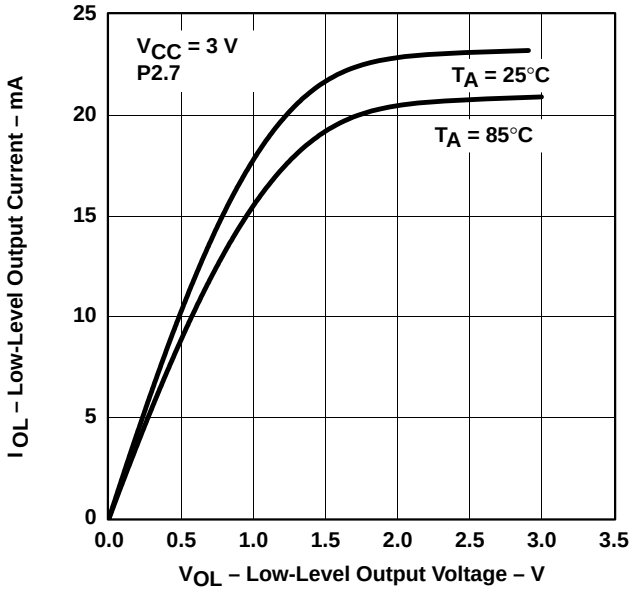


Figure 8

TYPICAL HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE

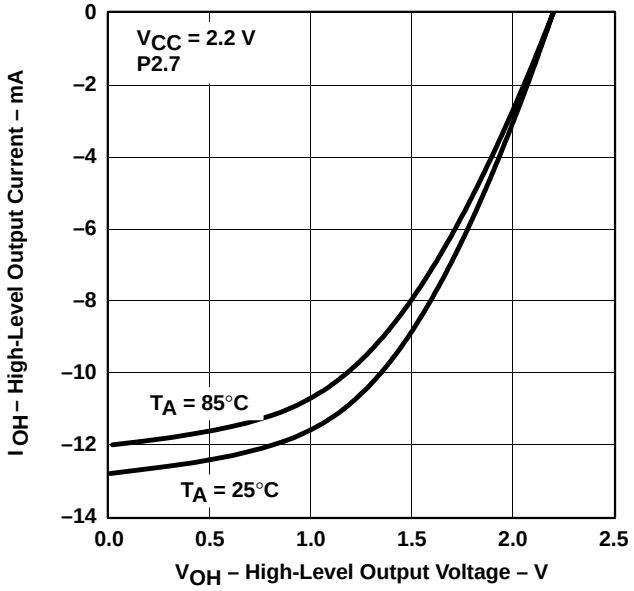


Figure 9

TYPICAL HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE

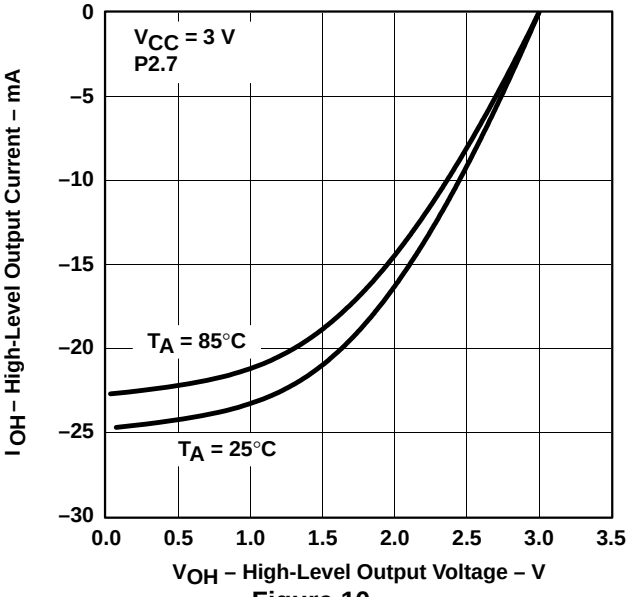


Figure 10

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

input frequency – Ports P1, P2, P3, P4, P5, and P6

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$f_{(IN)}$	Includes TACLK, TAINCLK, TBCLK	$t_{(h)} = t_{(L)}$	V_{CC} = 2.2 V			8	MHz
			V_{CC} = 3 V			10	

capture timing _ Timer_A3: TA0, TA1, TA2; Timer_B7: TB0 to TB6

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(int)}$	Ports P2, P4: External trigger signal for the interrupt flag (see Notes 1 and 2)	V_{CC} = 2.2 V/3 V	1.5			Cycle
		V_{CC} = 2.2 V	62			ns
		V_{CC} = 3 V	50			

NOTES: 1. The external signal sets the interrupt flag every time $t_{(int)}$ is met. It may be set even with trigger signals shorter than $t_{(int)}$. The conditions to set the flag must be met independently of this timing constraint. $t_{(int)}$ is defined in MCLK cycles.
2. The external signal needs additional timing because of the maximum input-frequency constraint.

output frequency

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{TAx}	TA0..2, TB0–TB6, Internal clock source, SMCLK signal applied (see Note 3)	C_L = 20 pF		DC		f_{System}	MHz
f_{ACLK}, f_{MCLK}, f_{SMCLK}	P5.6/ACLK, P5.4/MCLK, P5.5/SMCLK	C_L = 20 pF				f_{System}	
t_{Xdc}	Duty cycle of output frequency,	P2.0/ACLK C_L = 20 pF, V_{CC} = 2.2 V / 3 V	$f_{ACLK} = f_{LFXT1} = f_{XT1}$	40%		60%	
			$f_{ACLK} = f_{LFXT1} = f_{LF}$	30%		70%	
			$f_{ACLK} = f_{LFXT1/n}$		50%		
		P1.4/SMCLK, C_L = 20 pF, V_{CC} = 2.2 V / 3 V	$f_{SMCLK} = f_{LFXT1} = f_{XT1}$	40%		60%	
			$f_{SMCLK} = f_{LFXT1} = f_{LF}$	35%		65%	
			$f_{SMCLK} = f_{LFXT1/n}$	50%– 15 ns	50%	50%– 15 ns	
			$f_{SMCLK} = f_{DCOCLK}$	50%– 15 ns	50%	50%– 15 ns	

NOTE 3: The limits of the system clock MCLK has to be met; the system (MCLK) frequency should not exceed the limits. MCLK and SMCLK frequencies can be different.

external interrupt timing

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(int)}$	Ports P1, P2: External trigger signal for the interrupt flag (see Notes 4 and 5)	V_{CC} = 2.2 V/3 V	1.5			Cycle
		V_{CC} = 2.2 V	62			ns
		V_{CC} = 3 V	50			

NOTES: 4. The external signal sets the interrupt flag every time $t_{(int)}$ is met. It may be set even with trigger signals shorter than $t_{(int)}$. The conditions to set the flag must be met independently of this timing constraint. $t_{(int)}$ is defined in MCLK cycles.
5. The external signal needs additional timing because of the maximum input-frequency constraint.

wake-up LPM3

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(LPM3)}$	Delay time	V_{CC} = 2.2 V/3 V			6	µs

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

leakage current (see Note 1)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{lkg(P1.x)}$	Leakage current	Port P1	Port 1: $V_{(P1.x)}$ (see Note 2)	V_{CC} = 2.2 V/3 V			±50	nA
$I_{lkg(P2.x)}$		Port P2	Port 2: $V_{(P2.3)}$ $V_{(P2.4)}$ (see Note 2)				±50	
$I_{lkg(P6.x)}$		Port P6	Port 6: $V_{(P6.x)}$ (see Note 2)				±50	

NOTES: 1. The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
2. The port pin must be selected as input and there must be no optional pullup or pulldown resistor.

RAM

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VRAMh	CPU HALTED (see Note 3)	1.6			V

NOTE 3: This parameter defines the minimum supply voltage when the data in program memory RAM remain unchanged. No program execution should take place during this supply voltage condition.

Comparator_A (see Note 4)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{(DD)}$		CAON=1, CARSEL=0, CAREF=0	V_{CC} = 2.2 V		25	40	µA
			V_{CC} = 3 V		45	60	
$I_{(Refladder/Refdiode)}$		CAON=1, CARSEL=0, CAREF=1/2/3, no load at P2.3/CA0/TA1 and P2.4/CA1/TA2	V_{CC} = 2.2 V		30	50	µA
			V_{CC} = 3 V		45	71	
$V_{(IC)}$	Common-mode input voltage	CAON =1	V_{CC} = 2.2 V/3 V	0		V_{CC}–1	V
$V_{(Ref025)}$	$\frac{\text{Voltage @ 0.25 } V_{CC} \text{ node}}{V_{CC}}$	PCA0=1, CARSEL=1, CAREF=1, no load at P2.3/CA0/TA1 and P2.4/CA1/TA2	V_{CC} = 2.2 V/3 V	0.23	0.24	0.25	
$V_{(Ref050)}$	$\frac{\text{Voltage @ 0.5}V_{CC} \text{ node}}{V_{CC}}$	PCA0=1, CARSEL=1, CAREF=2, no load at P2.3/CA0/TA1 and P2.4/CA1/TA2	V_{CC} = 2.2 V/3 V	0.47	0.48	0.5	
$V_{(RefVT)}$	See Figure 12.	PCA0=1, CARSEL=1, CAREF=3, no load at P2.3/CA0/TA1 and P2.4/CA1/TA2 T_A = 85°C	V_{CC} = 2.2 V	390	480	540	mV
			V_{CC} = 3 V	400	490	550	
$V_{(offset)}$	Offset voltage	See Note 5	V_{CC} = 2.2 V/3 V	–30		30	mV
V_{hys}	Input hysteresis	CAON=1	V_{CC} = 2.2 V/3 V	0	0.7	1.4	mV
$t_{(response\ LH)}$		T_A = 25°C, Overdrive 10 mV, Without filter: CAF=0	V_{CC} = 2.2 V	130	210	300	ns
			V_{CC} = 3 V	80	150	240	
		T_A = 25°C, Overdrive 10 mV, With filter: CAF=1	V_{CC} = 2.2 V	1.4	1.9	3.4	µs
			V_{CC} = 3 V	0.9	1.5	2.6	
$t_{(response\ HL)}$		T_A = 25°C, Overdrive 10 mV, without filter: CAF=0	V_{CC} = 2.2 V	130	210	300	ns
			V_{CC} = 3 V	80	150	240	
		T_A = 25°C, Overdrive 10 mV, with filter: CAF=1	V_{CC} = 2.2 V	1.4	1.9	3.4	µs
			V_{CC} = 3 V	0.9	1.5	2.6	

NOTES: 4. The leakage current for the Comparator_A terminals is identical to $I_{lkg(Px.x)}$ specification.
5. The input offset voltage can be cancelled by using the CAEX bit to invert the Comparator_A inputs on successive measurements. The two successive measurements are then summed together.

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electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

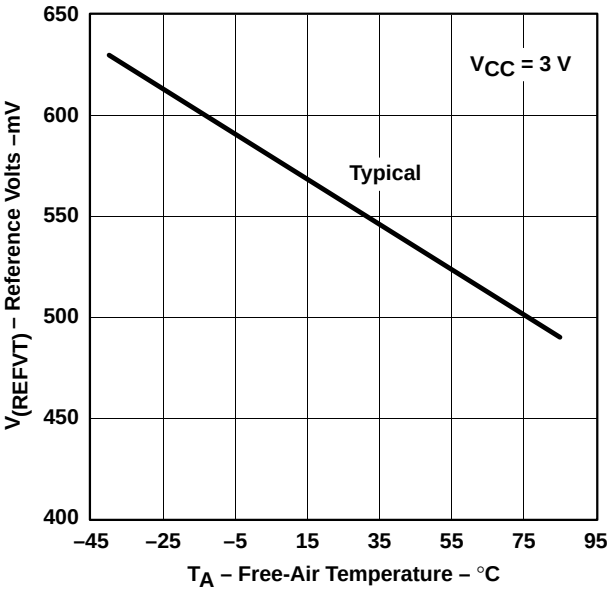

Figure 11. $V_{(RefVT)}$ vs Temperature, V_{CC} = 3 V

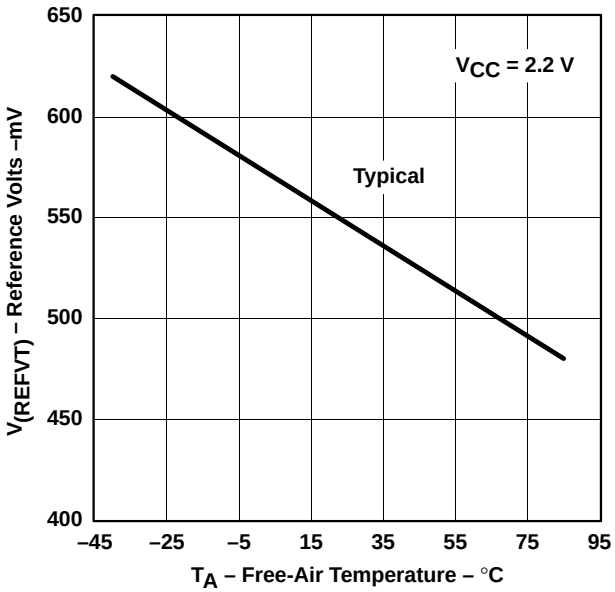

Figure 12. $V_{(RefVT)}$ vs Temperature, V_{CC} = 2.2 V

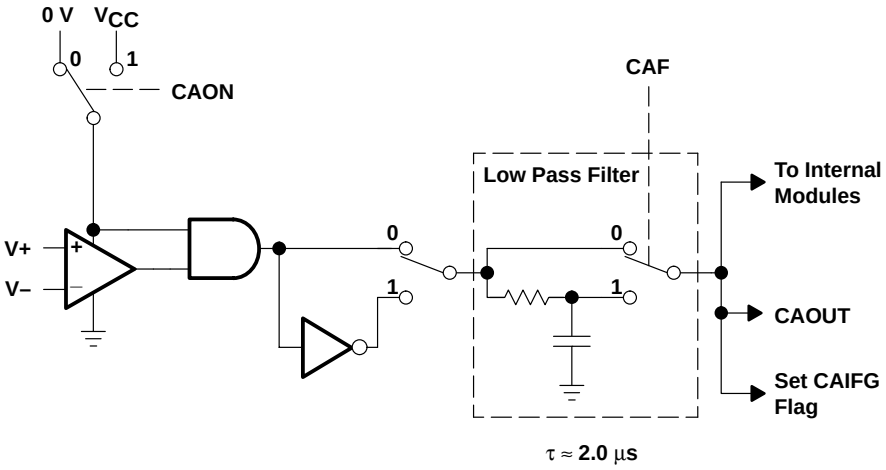

Figure 13. Block Diagram of Comparator_A Module

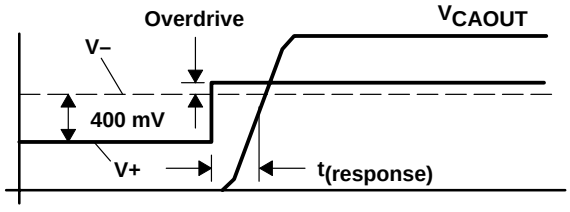

Figure 14. Overdrive Definition

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

POR/brownout reset (BOR) (see Notes 1 and 2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(BOR)}$	Brownout				2000	µs
$V_{CC(BOR)}$		$dV_{CC}/dt \le 3$ V/s (see Figure 15)		$0.7 \times V_{(B\_IT-)}$		V
$V_{(B\_IT-)}$		$dV_{CC}/dt \le 3$ V/s (see Figure 15 through Figure 17)			1.71	V
$V_{hys(B\_IT-)}$		$dV_{CC}/dt \le 3$ V/s (see Figure 15)	70	130	180	mV
$t_{(reset)}$		Pulse length needed at RST/NMI pin to accepted reset internally, V_{CC} = 2.2 V/3 V	2			µs

NOTES: 1. The current consumption of the brownout module is already included in the I_{CC} current consumption data. The voltage level $V_{(B\_IT-)} + V_{hys(B\_IT-)}$ is ≤ 1.8 V.

2. During power up, the CPU begins code execution following a period of $t_{BOR(delay)}$ after $V_{CC} = V_{(B\_IT-)} + V_{hys(B,IT-)}$. The default DCO settings must not be changed until $V_{CC} \ge V_{CC(min)}$. See the *MSP430x1xx Family User's Guide* for more information on the brownout/SVS circuit.

typical characteristics

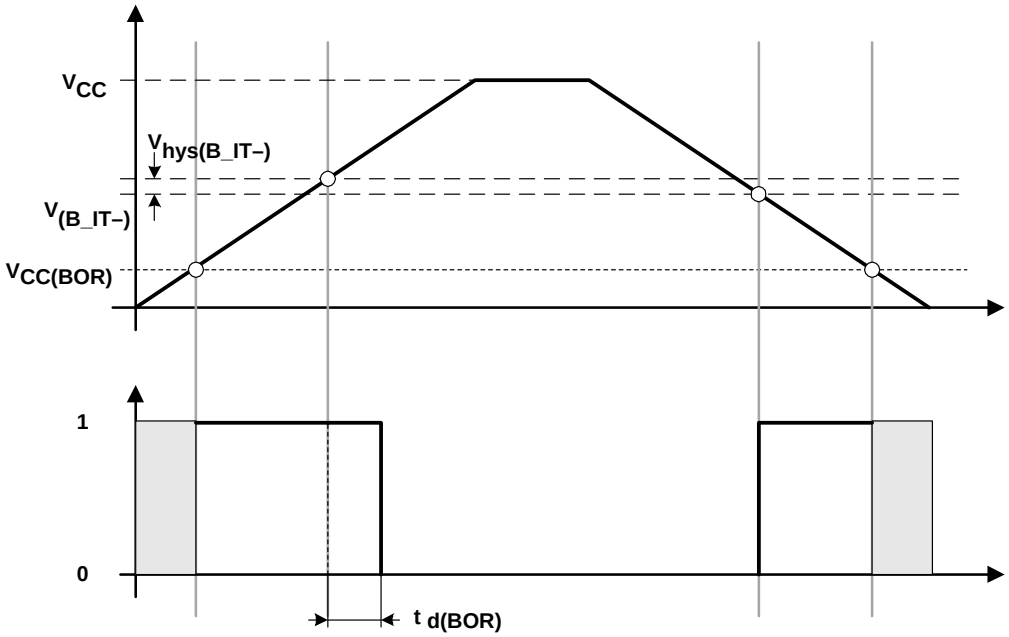

Figure 15. POR/Brownout Reset (BOR) vs Supply Voltage

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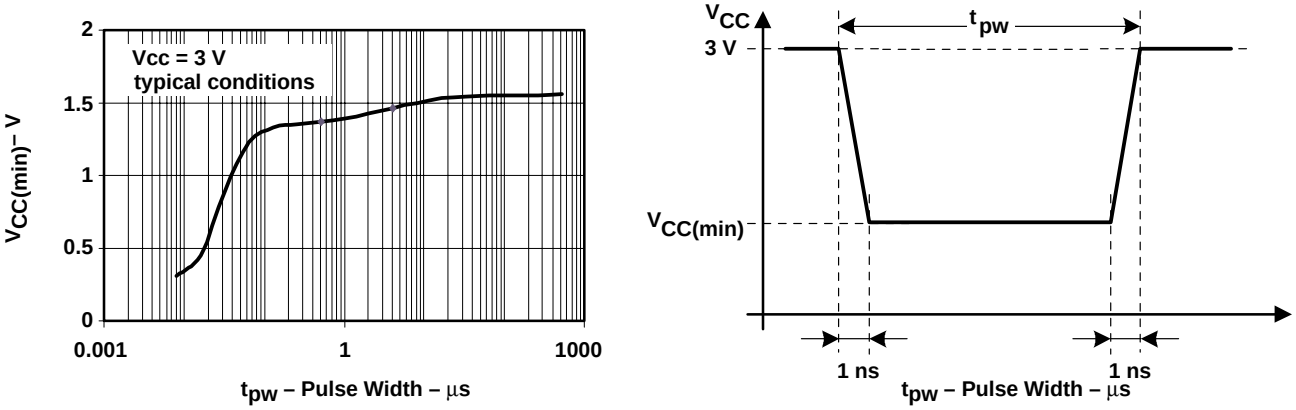

Figure 16. $V_{(CC)min}$ Level With a Square Voltage Drop to Generate a POR/Brownout Signal

typical characteristics

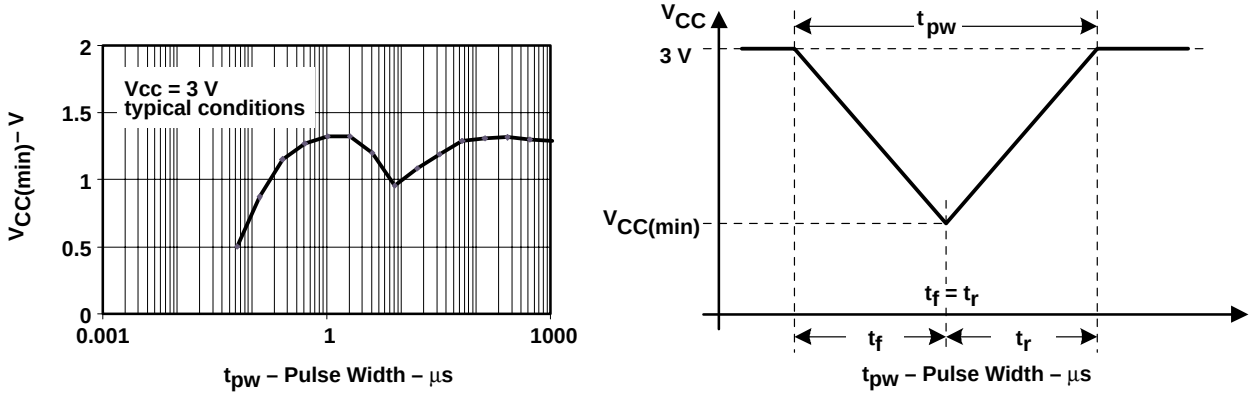

Figure 17. $V_{CC(min)}$ Level With a Triangle Voltage Drop to Generate a POR/Brownout Signal

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electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

SVS (supply voltage supervisor/monitor)

PARAMETER	TEST CONDITIONS		MIN	NOM	MAX	UNIT
$t_{(SVSR)}$	dV_{CC}/dt > 30 V/ms (see Figure 18)		5		150	µs
	$dV_{CC}/dt \le$ 30 V/ms				2000	µs
$t_{d(SVSon)}$	SVSon, switch from VLD = 0 to VLD ≠ 0, V_{CC} = 3 V		20		150	µs
t_{settle}	VLD ≠ 0‡				12	µs
$V_{(SVSstart)}$	VLD ≠ 0, $V_{CC}/dt \le$ 3 V/s (see Figure 18)			1.55	1.7	V
$V_{hys(B\_IT-)}$	$V_{CC}/dt \le$ 3 V/s (see Figure 18)	VLD = 1	70	120	155	mV
		VLD = 2 .. 14	$V_{(SVS\_IT-)}$ x 0.004		$V_{(SVS\_IT-)}$ x 0.008	
	$V_{CC}/dt \le$ 3 V/s (see Figure 18), External voltage applied on A7	VLD = 15	4.4		10.4	mV
$V_{(SVS\_IT-)}$	$V_{CC}/dt \le$ 3 V/s (see Figure 18 and Figure 19)	VLD = 1	1.8	1.9	2.05	V
		VLD = 2	1.94	2.1	2.25	
		VLD = 3	2.05	2.2	2.37	
		VLD = 4	2.14	2.3	2.48	
		VLD = 5	2.24	2.4	2.6	
		VLD = 6	2.33	2.5	2.71	
		VLD = 7	2.46	2.65	2.86	
		VLD = 8	2.58	2.8	3	
		VLD = 9	2.69	2.9	3.13	
		VLD = 10	2.83	3.05	3.29	
		VLD = 11	2.94	3.2	3.42	
		VLD = 12	3.11	3.35	3.61†	
		VLD = 13	3.24	3.5	3.76†	
		VLD = 14	3.43	3.7†	3.99†	
	$V_{CC}/dt \le$ 3 V/s (see Figure 18 and Figure 19), External voltage applied on A7	VLD = 15	1.1	1.2	1.3	
$I_{CC(SVS)}$ (see Note 1)	VLD ≠ 0, V_{CC} = 2.2 V/3 V			10	15	µA

† The recommended operating voltage range is limited to 3.6 V.

‡ t_{settle} is the settling time that the comparator o/p needs to have a stable level after VLD is switched VLD ≠ 0 to a different VLD value somewhere between 2 and 15. The overdrive is assumed to be > 50 mV.

NOTE 1: The current consumption of the SVS module is not included in the I_{CC} current consumption data.

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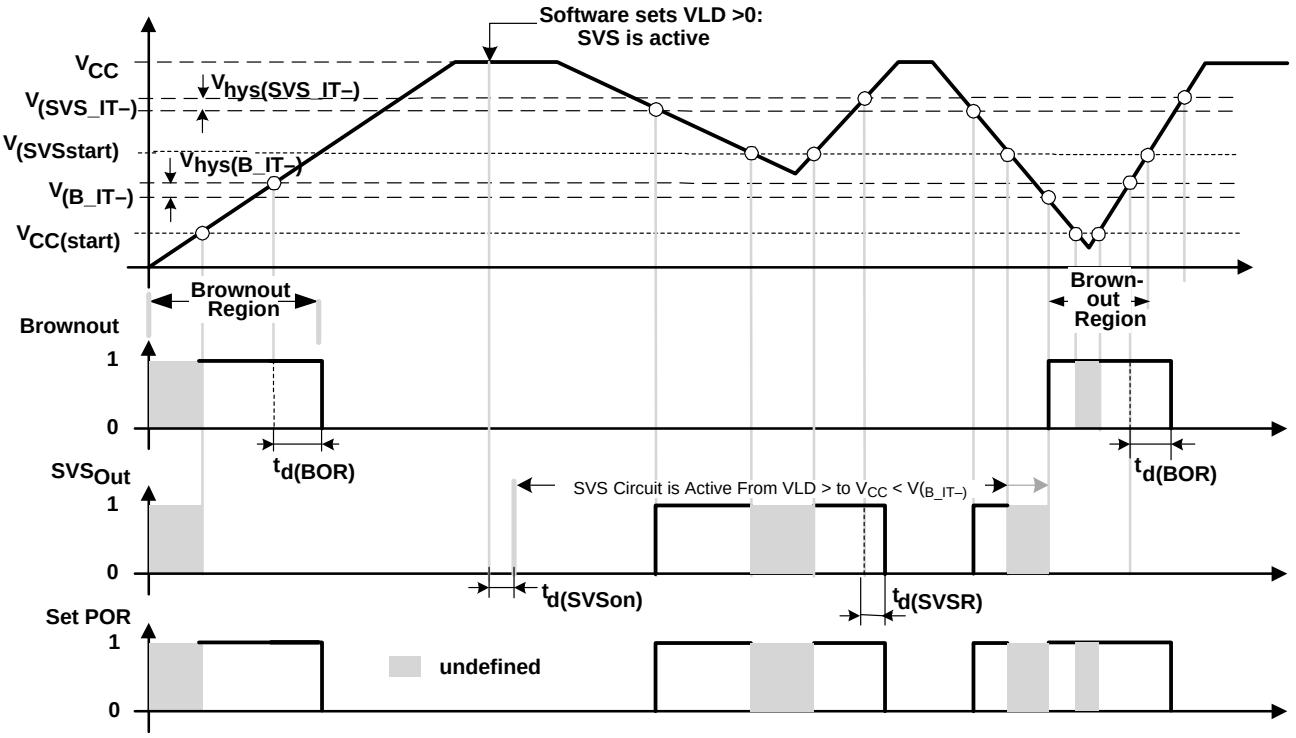

Figure 18. SVS Reset (SVSR) vs Supply Voltage

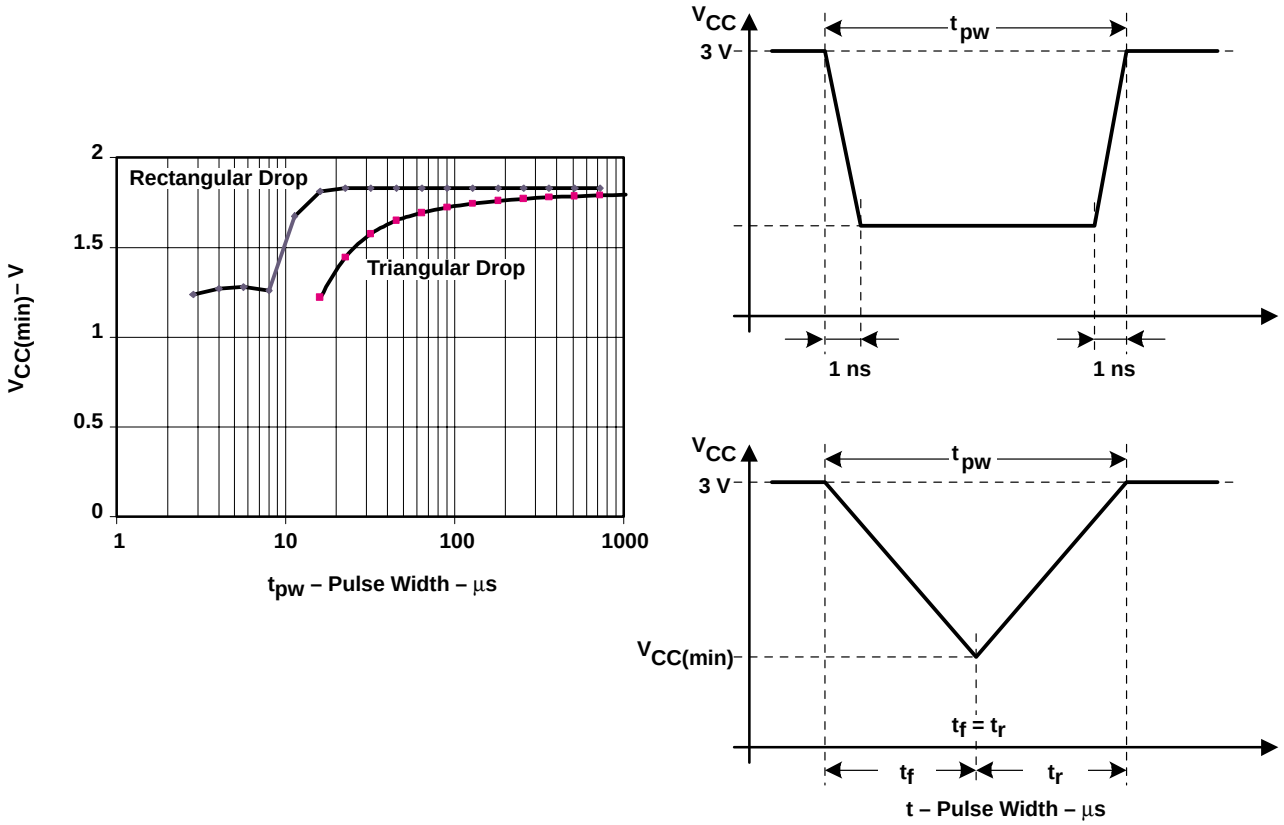

Figure 19. $V_{CC(min)}$ With a Square Voltage Drop and a Triangle Voltage Drop to Generate an SVS Signal

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

DCO (see Note 1)

PARAMETER	TEST CONDITIONS		MIN	NOM	MAX	UNIT
$f_{(DCO03)}$	R_{sel} = 0, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	0.08	0.12	0.15	MHz
		V_{CC} = 3 V	0.08	0.13	0.16	
$f_{(DCO13)}$	R_{sel} = 1, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	0.14	0.19	0.23	MHz
		V_{CC} = 3 V	0.14	0.18	0.22	
$f_{(DCO23)}$	R_{sel} = 2, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	0.22	0.30	0.36	MHz
		V_{CC} = 3 V	0.22	0.28	0.34	
$f_{(DCO33)}$	R_{sel} = 3, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	0.37	0.49	0.59	MHz
		V_{CC} = 3 V	0.37	0.47	0.56	
$f_{(DCO43)}$	R_{sel} = 4, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	0.61	0.77	0.93	MHz
		V_{CC} = 3 V	0.61	0.75	0.90	
$f_{(DCO53)}$	R_{sel} = 5, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	1	1.2	1.5	MHz
		V_{CC} = 3 V	1	1.3	1.5	
$f_{(DCO63)}$	R_{sel} = 6, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	1.6	1.9	2.2	MHz
		V_{CC} = 3 V	1.69	2.0	2.29	
$f_{(DCO73)}$	R_{sel} = 7, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	2.4	2.9	3.4	MHz
		V_{CC} = 3 V	2.7	3.2	3.65	
$f_{(DCO47)}$	R_{sel} = 4, DCO = 7, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V/3 V	$f_{DCO40} \times 1.7$	$f_{DCO40} \times 2.1$	$f_{DCO40} \times 2.5$	MHz
$f_{(DCO77)}$	R_{sel} = 7, DCO = 7, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	4	4.5	4.9	MHz
		V_{CC} = 3 V	4.4	4.9	5.4	
$S_{(Rsel)}$	$S_R = f_{Rsel+1} / f_{Rsel}$	V_{CC} = 2.2 V/3 V	1.35	1.65	2	
$S_{(DCO)}$	$S_{DCO} = f_{DCO+1} / f_{DCO}$	V_{CC} = 2.2 V/3 V	1.07	1.12	1.16	
D_t	Temperature drift, R_{sel} = 4, DCO = 3, MOD = 0 (see Note 2)	V_{CC} = 2.2 V	–0.31	–0.36	–0.40	%/°C
		V_{CC} = 3 V	–0.33	–0.38	–0.43	
D_V	Drift with V_{CC} variation, R_{sel} = 4, DCO = 3, MOD = 0 (see Note 2)	V_{CC} = 2.2 V/3 V	0	5	10	%/V

NOTES: 1. The DCO frequency may not exceed the maximum system frequency defined by parameter processor frequency, $f_{(System)}$.
2. This parameter is not production tested.

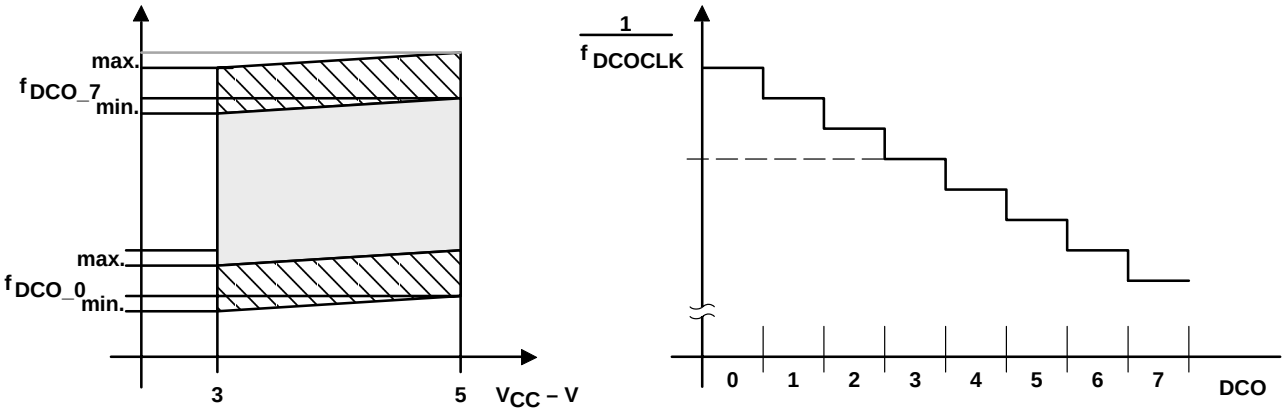

Figure 20. DCO Characteristics

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electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

main DCO characteristics

- Individual devices have a minimum and maximum operation frequency. The specified parameters for f_{DCOx0} to f_{DCOx7} are valid for all devices.
- All ranges selected by Rsel(n) overlap with Rsel(n+1): Rsel0 overlaps with Rsel1, ... Rsel6 overlaps with Rsel7.
- DCO control bits DCO0, DCO1, and DCO2 have a step size as defined by parameter S_{DCO}.
- Modulation control bits MOD0 to MOD4 select how often f_{DCO+1} is used within the period of 32 DCOCLK cycles. The frequency $f_{(DCO)}$ is used for the remaining cycles. The frequency is an average equal to $f_{(DCO)} \times (2^{MOD/32})$.

crystal oscillator, LFXT1 oscillator (see Note 1)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
X_{CIN}	Integrated input capacitance	XTS=0; LF oscillator selected, V_{CC} = 2.2 V/3 V		12		pF
		XTS=1; XT1 oscillator selected, V_{CC} = 2.2 V/3 V		2		
X_{COUT}	Integrated output capacitance	XTS=0; LF oscillator selected, V_{CC} = 2.2 V/3 V		12		pF
		XTS=1; XT1 oscillator selected, V_{CC} = 2.2 V/3 V		2		
X_{INL}	Input levels at XIN, XOUT	V_{CC} = 2.2 V/3 V	V_{SS}		$0.2 \times V_{CC}$	V
X_{INH}		V_{CC} = 2.2 V/3 V	$0.8 \times V_{CC}$		V_{CC}	V

NOTE 1: The oscillator needs capacitors at both terminals, with values specified by the crystal manufacturer.

crystal oscillator, XT2 oscillator (see Note 2)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
X_{CIN}	Integrated input capacitance	V_{CC} = 2.2 V/3 V		2		pF
X_{COUT}	Integrated output capacitance	V_{CC} = 2.2 V/3 V		2		pF
X_{INL}	Input levels at XIN, XOUT	V_{CC} = 2.2 V/3 V	V_{SS}		$0.2 \times V_{CC}$	V
X_{INH}		V_{CC} = 2.2 V/3 V	$0.8 \times V_{CC}$		V_{CC}	V

NOTE 2: The oscillator needs capacitors at both terminals, with values specified by the crystal manufacturer.

USART0, USART1 (see Note 3)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{(\tau)}$	USART0/USART1: deglitch time	V_{CC} = 2.2 V	200	430	800	ns
		V_{CC} = 3 V	150	280	500	

NOTE 3: The signal applied to the USART0/USART1 receive signal/terminal (URXD0/1) should meet the timing requirements of $t_{(t)}$ to ensure that the URXS flip-flop is set. The URXS flip-flop is set with negative pulses meeting the minimum-timing condition of $t_{(t)}$. The operating conditions to set the flag must be met independently from this timing constraint. The deglitch circuitry is active only on negative transitions on the URXD0/1 line.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit ADC, power supply and input range conditions (see Note 1)

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
AV_{CC}	Analog supply voltage	AV_{CC} and DV_{CC} are connected together AV_{SS} and DV_{SS} are connected together $V_{(AVSS)} = V_{(DVSS)} = 0$ V		2.2		3.6	V
V_{REF+}	Positive built-in reference voltage output	2_5 V = 1 for 2.5 V built-in reference 2_5 V = 0 for 1.5 V built-in reference $I_{V(REF+)} \leq I_{(VREF+)}max$	3 V	2.4	2.5	2.6	V
			2.2 V/3 V	1.44	1.5	1.56	
I_{VREF+}	Load current out of V_{REF+} terminal		2.2 V	0.01		–0.5	mA
			3 V			–1	
$I_{L(VREF)+}$	Load-current regulation V_{REF+} terminal	$I_{V(REF)+}$ = 500 µA +/– 100 µA Analog input voltage ~0.75 V; 2_5 V = 0	2.2 V			±2	LSB
			3 V			±2	
		$I_{V(REF)+}$ = 500 µA ± 100 µA Analog input voltage ~1.25 V; 2_5 V = 1	3 V			±2	LSB
$I_{DL(VREF)+}$	Load current regulation V_{REF+} terminal	$I_{V(REF)+}$ =100 µA → 900 µA, VCC=3 V, ax ~0.5 x V_{REF+} Error of conversion result ≤ 1 LSB	C_{VREF+}=5 µF			20	ns
V_{eREF+}	Positive external reference voltage input	$V_{eREF+} > V_{eREF–}/V_{eREF–}$ (see Note 2)		1.4		V_{AVCC}	V
$V_{REF–}$ /$V_{eREF–}$	Negative external reference voltage input	$V_{eREF+} > V_{eREF–}/V_{eREF–}$ (see Note 3)		0		1.2	V
(V_{eREF+} – $V_{REF–}/V_{eREF–}$)	Differential external reference voltage input	$V_{eREF+} > V_{eREF–}/V_{eREF–}$ (see Note 4)		1.4		V_{AVCC}	V
$V_{(P6.x/Ax)}$	Analog input voltage range (see Note 5)	All P6.0/A0 to P6.7/A7 terminals. Analog inputs selected in ADC12MCTLx register and P6Sel.x=1 $0 \leq x \leq 7$; $V_{(AVSS)} \leq V_{P6.x/Ax} \leq V_{(AVCC)}$		0		V_{AVCC}	V
I_{ADC12}	Operating supply current into AV_{CC} terminal (see Note 6)	$f_{ADC12CLK}$ = 5.0 MHz ADC12ON = 1, REFON = 0 SHT0=0, SHT1=0, ADC12DIV=0	2.2 V		0.65	1.3	mA
			3 V		0.8	1.6	
I_{REF+}	Operating supply current into AV_{CC} terminal (see Note 7)	$f_{ADC12CLK}$ = 5.0 MHz ADC12ON = 0, REFON = 1, 2_5V = 1	3 V		0.5	0.8	mA
I_{REF+}	Operating supply current (see Note 7)	$f_{ADC12CLK}$ = 5.0 MHz ADC12ON = 0, REFON = 1, 2_5V = 0	2.2 V		0.5	0.8	mA
			3 V		0.5	0.8	

NOTES:
1. The leakage current is defined in the leakage current table with P6.x/Ax parameter.
2. The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
3. The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
4. The accuracy limits minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.
5. The analog input voltage range must be within the selected reference voltage range V_{R+} to $V_{R–}$ for valid conversion results.
6. The internal reference supply current is not included in current consumption parameter I_{ADC12}.
7. The internal reference current is supplied via terminal AV_{CC}. Consumption is independent of the ADC12ON control bit, unless a conversion is active. The REFON bit enables to settle the built-in reference before starting an A/D conversion.

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electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit ADC, built-in reference (see Note 1)

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
I_{VeREF+}	Static input current (see Note 2)	$0V \le V_{eREF+} \le V_{AVCC}$	2.2 V/3 V			±1	µA
$I_{VREF-/VeREF-}$	Static input current (see Note 2)	$0V \le V_{eREF-} \le V_{AVCC}$	2.2 V/3 V			±1	µA
C_{VREF+}	Capacitance at pin V_{REF+} (see Note 3)	REFON =1, $0 mA \le I_{VREF+} \le I_{V(REF)+(max)}$	2.2 V/3 V	5	10		µF
C_i	Input capacitance (see Note 4)	Only one terminal can be selected at one time, P6.x/Ax	2.2 V			40	pF
Z_i	Input MUX ON resistance(see Note 4)	$0V \le V_{Ax} \le V_{AVCC}$	3 V			2000	Ω
T_{REF+}	Temperature coefficient of built-in reference	$I_{V(REF)+}$ is a constant in the range of $0 mA \le I_{V(REF)+} \le 1 mA$	2.2 V/3 V			±100	ppm/°C

NOTES: 1. The voltage source on V_{eREF+} and V_{REF-}/V_{eREF-}) needs to have low dynamic impedance for 12-bit accuracy to allow the charge to settle for this accuracy (See Figures 12 and 13).
2. The external reference is used during conversion to charge and discharge the capacitance array. The dynamic impedance should follow the recommendations on analog-source impedance to allow the charge to settle for 12-bit accuracy.
3. The internal buffer operational amplifier and the accuracy specifications require an external capacitor.
4. The input capacitance is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 12-bit accuracy. All INL and DNL tests uses two capacitors between pins V(REF+) and AVSS and V(REF–)/V(eREF–) and AVSS: 10 µF tantalum and 100 nF ceramic.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit ADC, timing parameters

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
$t_{REF(ON)}$	Settle time of internal reference voltage (see Figure 21 and Note 1)	$I_{V(REF)+}$ = 0.5 mA, $C_{V(REF)+}$ = 10 μF, V_{REF+} = 1.5 V, V_{AVCC} = 2.2 V				17	ms
f(ADC12OSC)		ADC12DIV=0 [f(ADC12CLK) =f(ADC12OSC)]	2.2 V	3.7		6.3	MHz
			3 V				
$t_{CONVERT}$	Conversion time	$AV_{CC(min)} \le V_{AVCC} \le AV_{CC(max)}$, $C_{VREF+} \ge 5$ μF, Internal oscillator, f_{OSC} = 3.7 MHz to 6.3 MHz	2.2 V/ 3 V	2.06		3.51	μs
	Conversion time	$A_{VCC(min)} \le V_{AVCC} \le A_{VCC(max)}$, External $f_{ADC12(CLK)}$ from ACLK or MCLK or SMCLK: ADC12SSEL ≠ 0			13×ADC12DIV× $1/f_{ADC12(CLK)}$		μs
$t_{ADC12ON}$	Settle time of the ADC	$A_{VCC(min)} \le V_{AVCC} \le A_{VCC(max)}$ (see Note 2)				100	ns
t_{Sample}	Sampling time	$V_{AVCC(min)} \le V_{AVCC} \le V_{AVCC(max)}$ $R_{i(source)}$ = 400 Ω, Z_i = 1000 Ω, C_i = 30 pF $\tau = [R_{i(source)} \times + Z_i] \times C_i$ (see Note 3)	3 V	1220			ns
			2.2 V	1400			

NOTES: 1. The condition is that the error in a conversion started after $t_{REF(ON)}$ is less than ±0.5 LSB. The settling time depends on the external capacitive load.
2. The condition is that the error in a conversion started after $t_{ADC12ON}$ is less than ±0.5 LSB. The reference and input signal are already settled.
3. Ten Tau (τ) are needed to get an error of less than ±0.5 LSB. t_{Sample} = 10 x (Ri + Zi) x Ci+ 800 ns

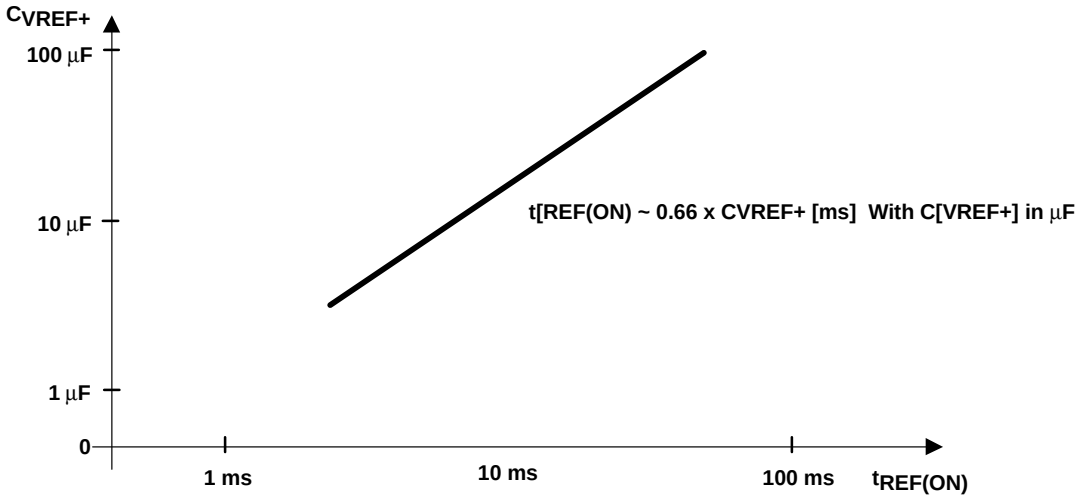

Figure 21. Typical Settling Time of Internal Reference $t_{REF(ON)}$ vs External Capacitor on V_{REF+}

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit ADC, linearity parameters

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
$E_{(I)}$	Integral linearity error	1.4 V ≤ (VeREF+ – VREF–/VeREF–) min ≤ 1.6 V	2.2 V/3 V			±2	LSB
		1.6 V < [V(eREF+) – V(REF–)/V(eREF–)] min ≤ [V(AVCC)]				±1.7	
E_D	Differential linearity error	$(V_{eREF+} - V_{REF-}/V_{eREF-})_{min} \le (V_{eREF+} - V_{REF-}/V_{eREF-})$, C(VREF+) = 10 µF (tantalum) and 100 nF (ceramic)	2.2 V/3 V			±1	LSB
E_O	Offset error	$(V_{eREF+} - V_{REF-}/V_{eREF-})_{min} \le (V_{eREF+} - V_{REF-}/V_{eREF-})$, Internal impedance of source R_i < 100 Ω, C(VREF+) = 10 µF (tantalum) and 100 nF (ceramic)	2.2 V/3 V		±2	±4	LSB
E_G	Gain error	$(V_{eREF+} - V_{REF-}/V_{eREF-})_{min} \le (V_{eREF+} - V_{REF-}/V_{eREF-})$, C(VREF+) = 10 µF (tantalum) and 100 nF (ceramic)	2.2 V/3 V		±1.1	±2	LSB
E_T	Total unadjusted error†	$(V_{eREF+} - V_{REF-}/V_{eREF-})_{min} \le (V_{eREF+} - V_{REF-}/V_{eREF-})$, C(VREF+) = 10 µF (tantalum) and 100 nF (ceramic)	2.2 V/3 V		±2	±5	LSB

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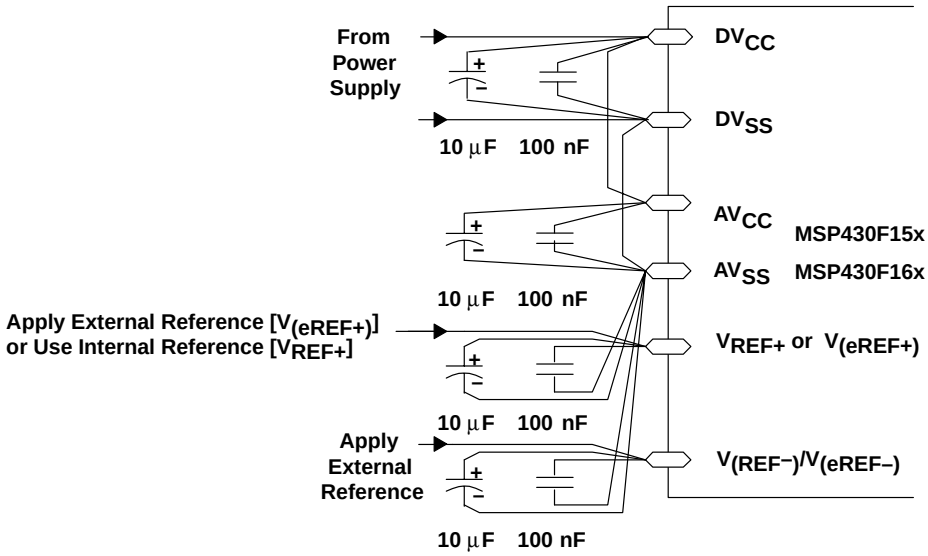

Figure 22. Supply Voltage and Reference Voltage Design $V_{(REF-)}/V_{(eREF-)}$ External Supply

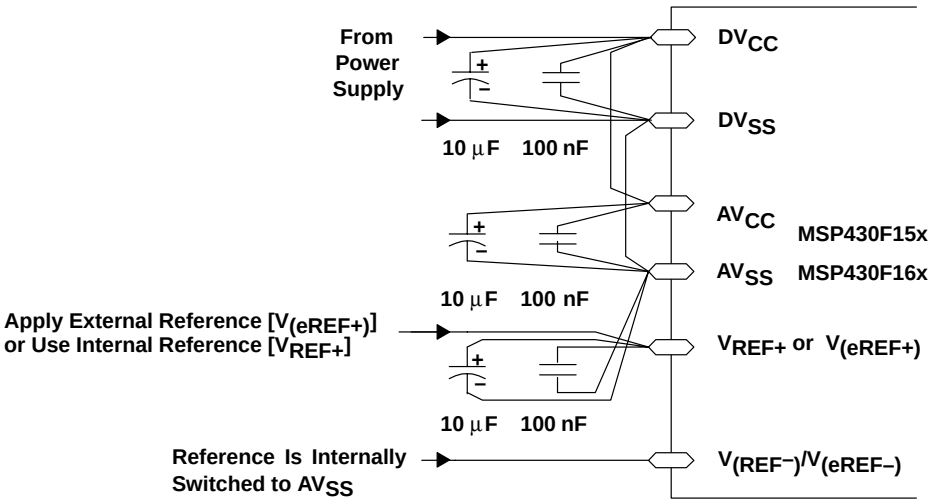

Figure 23. Supply Voltage and Reference Voltage Design $V_{(REF-)}/V_{(eREF-)}$ =AV_{SS}, Internally Connected

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit ADC, temperature sensor and built-in Vmid

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
I_{SENSOR}	Operating supply current into AV_{CC} terminal (see Note 1)	V_{REFON} = 0, INCH = 0Ah, ADC12ON=NA, T_A = 25°C	2.2 V		40	120	µA
			3 V		60	160	
V_{SENSOR}		ADC12ON = 1, INCH = 0Ah, T_A = 0°C	2.2 V		986	986±5%	mV
			3 V		986	986±5%	
TC_{SENSOR}		ADC12ON = 1, INCH = 0Ah	2.2 V		3.55	3.55±3%	mV/°C
			3 V		3.55	3.55±3%	
$t_{SENSOR(sample)}$	Sample time required if channel 10 is selected (see Note 2)	ADC12ON = 1, INCH = 0Ah, Error of conversion result ≤ 1 LSB	2.2 V	30			µs
			3 V	30			
I_{VMID}	Current into divider at channel 11	ADC12ON = 1, INCH = 0Bh, (see Note 3)	2.2 V			NA	µA
			3 V			NA	
V_{MID}	AV_{CC} divider at channel 11	ADC12ON = 1, INCH = 0Bh, V_{MID} is ~0.5 x V_{AVCC}	2.2 V		1.1	1.1±0.04	V
			3 V		1.5	1.50±0.04	
$t_{ON(VMID)}$	On-time if channel 11 is selected (see Note 4)	ADC12ON = 1, INCH = 0Bh, Error of conversion result ≤ 1 LSB	2.2 V			NA	ns
			3 V			NA	

NOTES: 1. The sensor current I_{SENSOR} is consumed if (ADC12ON = 1 and V_{REFON}=1), or (ADC12ON=1 AND INCH=0Ah and sample signal is high). Therefore it includes the constant current through the sensor and the reference.
2. The typical equivalent impedance of the sensor is 51 kΩ. The sample time needed is the sensor-on time $t_{SENSOR(ON)}$
3. No additional current is needed. The V_{MID} is used during sampling.
4. The on-time $t_{ON(VMID)}$ is identical to sampling time t_{Sample}; no additional on time is needed.

DAC12 specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution	R_L = 10 kΩ, C_L = 100 pF		12		bits
INL	Integral nonlinearity	R_L = 10 kΩ, C_L = 100 pF, see Note 5		±1.9	±4	LSB
DNL	Differential nonlinearity	R_L = 10 kΩ, C_L = 100 pF, see Note 6		±0.5	±1	LSB
E_{ZS}	Zero-scale error (offset error at zero scale)	R_L = 10 kΩ, C_L = 100 pF, see Note 7			±10	mV
	Zero-scale-error temperature coefficient	R_L = 10 kΩ, C_L = 100 pF, see Note 8		10		ppm/°C
E_G	Gain error	R_L = 10 kΩ, C_L = 100 pF, see Note 9			±0.6	% of FS voltage
	Gain-error temperature coefficient	R_L = 10 kΩ, C_L = 100 pF, see Note 10		10		ppm/°C
V_O	Voltage output range	R_L = 10 kΩ	0		AV_{DD}–0.1	V
		R_L = ∞			TBD	
R_L	DAC12 load resistance, $R_{L(DAC12.x)}$		2			kΩ
C_L	DAC12 load capacitance, $C_{L(DAC12.x)}$				100	pF

NOTES: 5. The relative accuracy or integral nonlinearity (INL) sometimes referred to as linearity error, is the maximum deviation of the output from the line between zero and full scale excluding the effects of zero code and full-scale errors.
6. The differential nonlinearity (DNL) sometimes referred to as differential error, is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.
7. Zero-scale error is the deviation from zero voltage output when the digital input code is zero.
8. Zero-scale-error temperature coefficient is given by: E_{ZS} TC = $[E_{ZS}(T_{max}) – E_{ZS}(T_{min})]/V_{ref} \times 10^6/(T_{max} – T_{min})$.
9. Gain error is the deviation from the ideal output ($2V_{ref}$ – 1 LSB) with an output load of 10 kΩ excluding the effects of the zero-error.
10. Gain temperature coefficient is given by: E_G TC = $[E_G(T_{max}) – E_G(T_{min})]/V_{ref} \times 10^6/(T_{max} – T_{min})$.

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DAC12 specifications (continued)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Output load regulation accuracy	R_L = 2 kΩ, vs 10 kΩ			0.1	±0.25	% of FS voltage
$t_{s(FS)}$	Output settling time, full scale	R_L = 10 kΩ, C_L = 100 pF, See Note 1	Fast		3	5.5	µs
			Slow		9	20	
$t_{s(CC)}$	Output settling time, code to code	R_L = 10 kΩ, C_L = 100 pF, See Note 2	Fast		1		µs
			Slow		2		µs
SR	Slew rate	R_L = 10 kΩ, C_L = 100 pF, See Note 3	Fast		3.6		V/µs
			Slow		0.9		
	Glitch energy	Code transition from 0x7FF to 0x800			10		nV–s
S/N	Signal to noise	fs = 400 KSPS, fout = 1.1 kHz, R_L = 10 kΩ, C_L = 100 pF, BW = 20 kHz			74		dB
S/(N+D)	Signal to noise + distortion				66		dB
THD	Total harmonic distortion				–68		dB
	Spurious free dynamic range				70		dB
I_{DD}	Power supply current	V_{DD} = 5 V, VREF = 2.048 V, No load, All inputs = AGND or V_{DD}, DAC latch = 0x800	Fast		TBD	TBD	µA
			Slow		TBD	TBD	µA
		V_{DD} = 3 V, VREF = 1.024 V No load, All inputs = AGND or V_{DD}, DAC latch = 0x800	Fast		TBD	TBD	µA
			Slow		TBD	TBD	µA
PSRR	Power supply rejection ratio	Zero scale, See Note 4			–80		dB
		Full scale, See Note 5			–80		

1. Settling time is the time for the output signal to remain within ±0.5 LSB of the final measured value for a digital input code change of 0x080 to 0x3FF or 0x3FF to 0x080. Not tested, ensured by design.
2. Settling time is the time for the output signal to remain within ± 0.5 LSB of the final measured value for a digital input code change of one count. Code change from 0x1FF to 0x200. Not tested, ensured by design.
3. Slew rate determines the time it takes for a change of the DAC output from 10% to 90% full-scale voltage.
4. Power supply rejection ratio at zero scale is measured by varying V_{DD} and is given by:
   $PSRR = 20 \log [(E_{ZS}(V_{DD}max) – E_{ZS}(V_{DD}min))/V_{DD}max]$
5. Power supply rejection ratio at full scale is measured by varying V_{DD} and is given by:
   $PSRR = 20 \log [(E_G(V_{DD}max) – E_G(V_{DD}min))/V_{DD}max]$

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JTAG, program memory and fuse

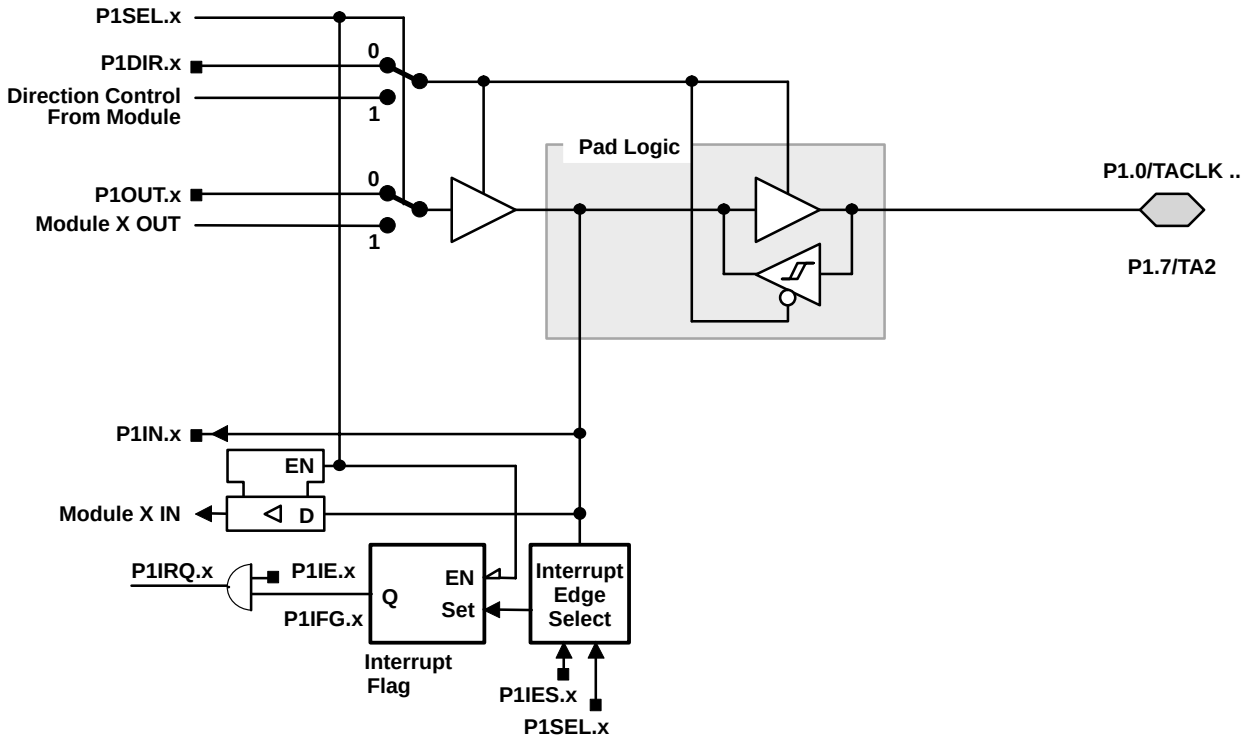
PARAMETER		TEST CONDITIONS	V_{CC}	MIN	NOM	MAX	UNIT
$f_{(TCK)}$	JTAG/Test (see Note 4)	TCK frequency	2.2 V	DC		5	MHz
			3 V	DC		10	
		Pullup resistors on TMS, TCK, TDI (see Note 1)	2.2 V/ 3V	25	60	90	kΩ
$V_{CC(FB)}$	JTAG/fuse (see Note 2)	Supply voltage during fuse-blow condition, $T_{(A)}$ = 25°C		2.5			V
V_{FB}		Fuse-blow voltage, F versions (see Note 3)		6.0		7.0	V
I_{FB}		Supply current on TDI with fuse blown				100	mA
		Time to blow the fuse				1	ms
$I_{(DD-PGM)}$	F-versions only (see Note 4)	Current from DV_{CC} when programming is active	2.7 V/3.6 V		3	5	mA
$I_{(DD-Erase)}$		Current from DV_{CC} when erase is active	2.7 V/3.6 V		3	5	mA
$t_{(retention)}$	F-versions only	Write/erase cycles		10^4	10^5		cycles
		Data retention T_J = 25°C		100			years

NOTES: 1. TMS, TDI, and TCK pullup resistors are implemented in all F versions.
2. Once the fuse is blown, no further access to the MSP430 JTAG/test feature is possible. The JTAG block is switched to bypass mode.
3. The supply voltage to blow the fuse is applied to the TDI pin.
4. $f_{(TCK)}$ may be restricted to meet the timing requirements of the module selected. Duration of the program/erase cycle is determined by $f_{(FTG)}$ applied to the flash timing controller. It can be calculated as follows:

$t_{(word\ write)} = 35 \times 1/f_{(FTG)}$
$t_{(block\ write,\ byte\ 0)} = 30 \times 1/f_{(FTG)}$
$t_{(block\ write,\ bytes\ 1–63)} = 20 \times 1/f_{(FTG)}$
$t_{(block\ write\ end\ sequence)} = 6 \times 1/f_{(FTG)}$
$t_{(mass\ erase)} = 5297 \times 1/f_{(FTG)}$
$t_{(segment\ erase)} = 4819 \times 1/f_{(FTG)}$

input/output schematic

port P1, P1.0 to P1.7, input/output with Schmitt-trigger

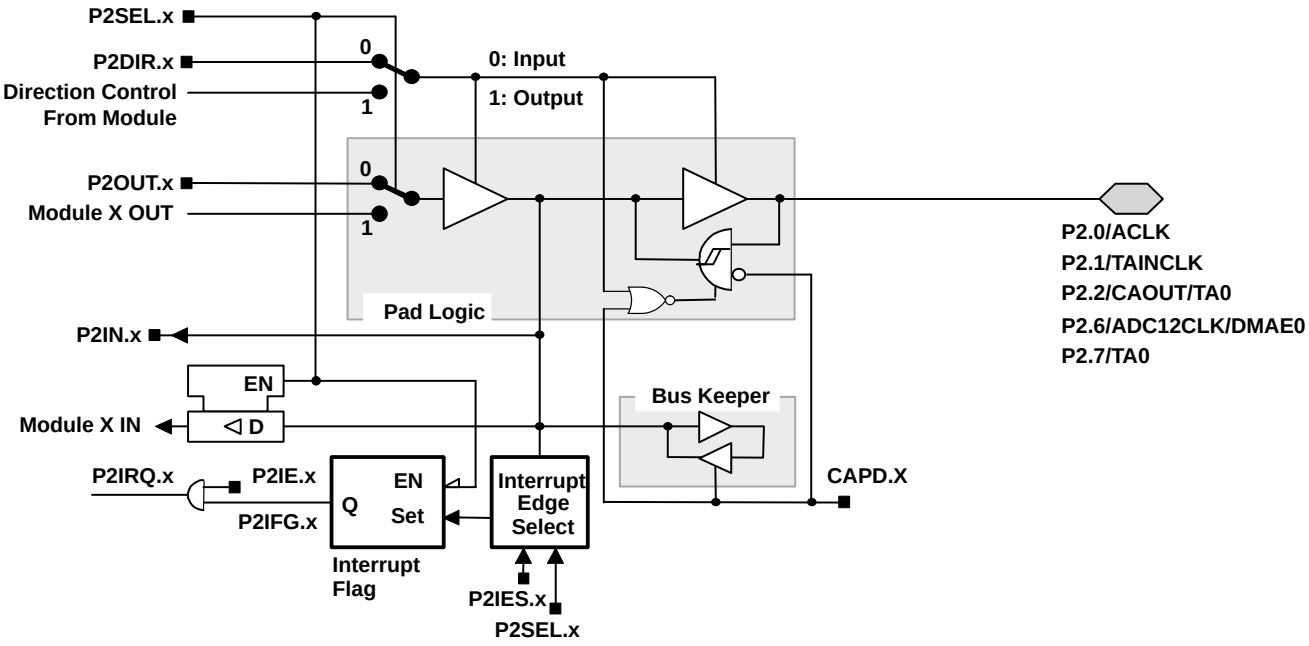


PnSel.x	PnDIR.x	Dir. CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN	PnIE.x	PnIFG.x	PnIES.x
P1Sel.0	P1DIR.0	P1DIR.0	P1OUT.0	DV_{SS}	P1IN.0	TACLK†	P1IE.0	P1IFG.0	P1IES.0
P1Sel.1	P1DIR.1	P1DIR.1	P1OUT.1	Out0 signal†	P1IN.1	CCI0A†	P1IE.1	P1IFG.1	P1IES.1
P1Sel.2	P1DIR.2	P1DIR.2	P1OUT.2	Out1 signal†	P1IN.2	CCI1A†	P1IE.2	P1IFG.2	P1IES.2
P1Sel.3	P1DIR.3	P1DIR.3	P1OUT.3	Out2 signal†	P1IN.3	CCI2A†	P1IE.3	P1IFG.3	P1IES.3
P1Sel.4	P1DIR.4	P1DIR.4	P1OUT.4	SMCLK	P1IN.4	unused	P1IE.4	P1IFG.4	P1IES.4
P1Sel.5	P1DIR.5	P1DIR.5	P1OUT.5	Out0 signal†	P1IN.5	unused	P1IE.5	P1IFG.5	P1IES.5
P1Sel.6	P1DIR.6	P1DIR.6	P1OUT.6	Out1 signal†	P1IN.6	unused	P1IE.6	P1IFG.6	P1IES.6
P1Sel.7	P1DIR.7	P1DIR.7	P1OUT.7	Out2 signal†	P1IN.7	unused	P1IE.7	P1IFG.7	P1IES.7

† Signal from or to Timer_A

input/output schematic (continued)

port P2, P2.0 to P2.2, P2.6, and P2.7 input/output with Schmitt-trigger



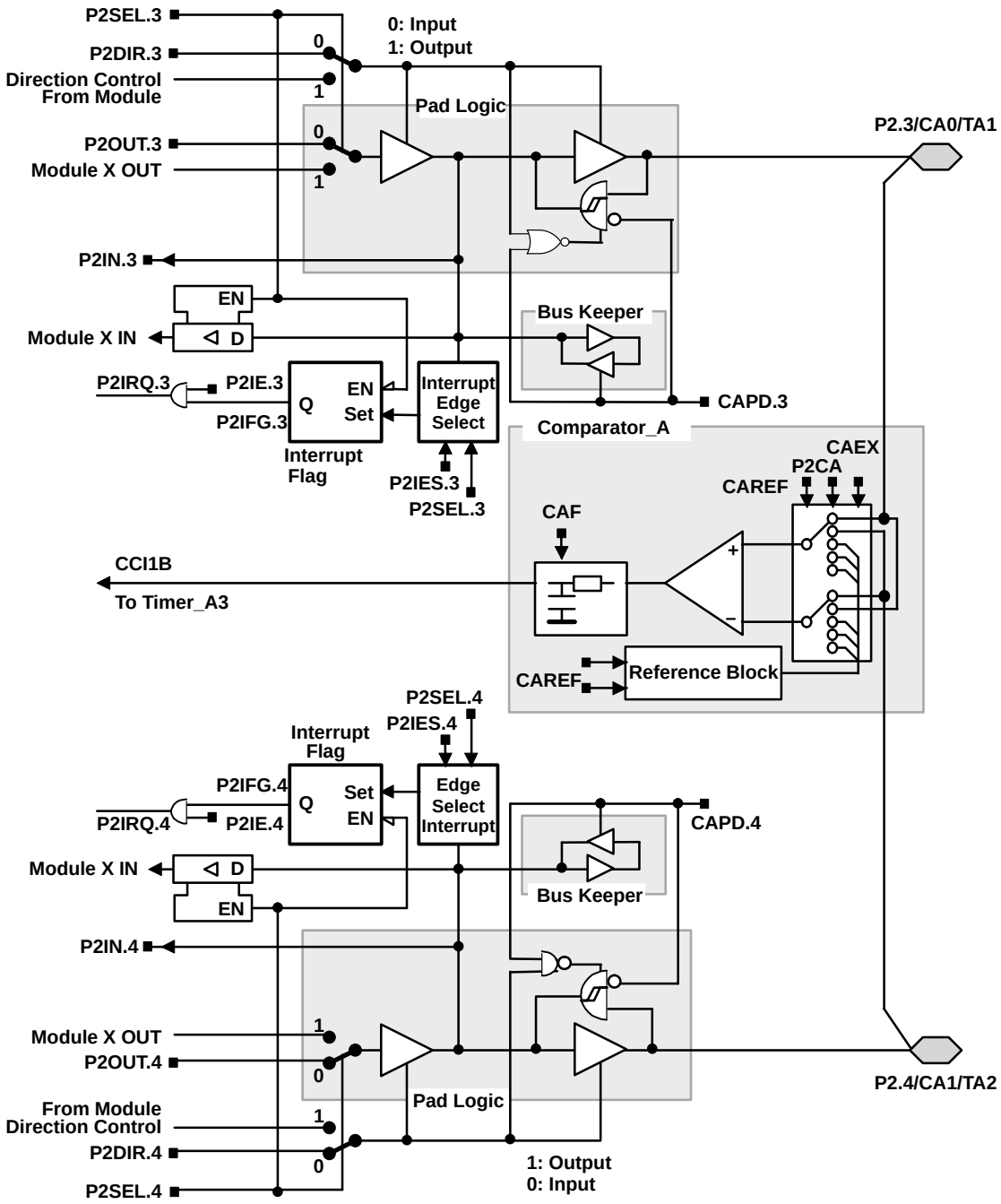
x: Bit Identifier 0 to 2, 6, and 7 for Port P2

PnSel.x	PnDIR.x	Dir. CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN	PnIE.x	PnIFG.x	PnIES.x
P2Sel.0	P2DIR.0	P2DIR.0	P2OUT.0	ACLK	P2IN.0	unused	P2IE.0	P2IFG.0	P2IES.0
P2Sel.1	P2DIR.1	P2DIR.1	P2OUT.1	DV_{SS}	P2IN.1	INCLK‡	P2IE.1	P2IFG.1	P2IES.1
P2Sel.2	P2DIR.2	P2DIR.2	P2OUT.2	CAOUT†	P2IN.2	CCI0B‡	P2IE.2	P2IFG.2	P2IES.2
P2Sel.6	P2DIR.6	P2DIR.6	P2OUT.6	ADC12CLK¶	P2IN.6	DMAE0#	P2IE.6	P2IFG.6	P2IES.6
P2Sel.7	P2DIR.7	P2DIR.7	P2OUT.7	Out0 signal§	P2IN.7	unused	P2IE.7	P2IFG.7	P2IES.7

† Signal from Comparator_A
‡ Signal to Timer_A
§ Signal from Timer_A
¶ ADC12CLK signal is output of the 12-bit ADC module
# Signal to DMA, channel 0

input/output schematic (continued)

port P2, P2.3 to P2.4, input/output with Schmitt-trigger

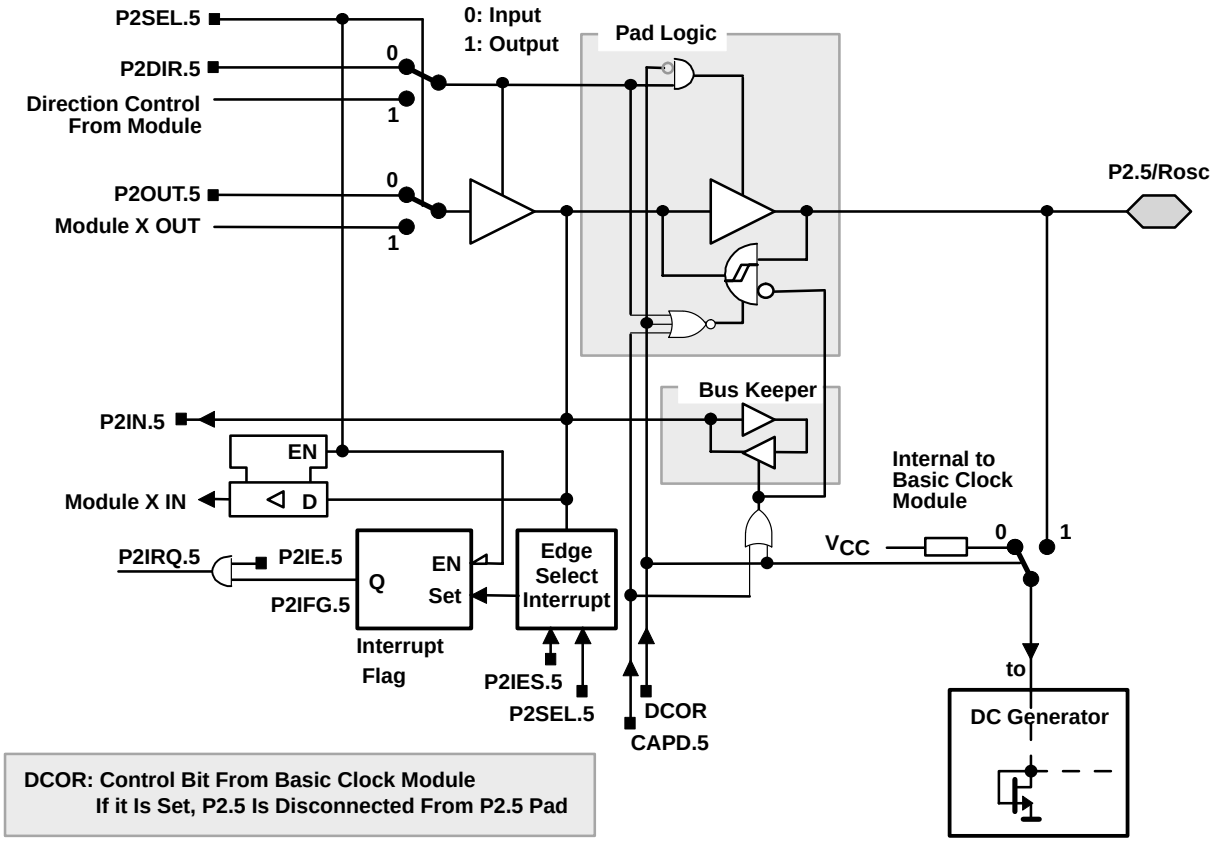


PnSel.x	PnDIR.x	DIRECTION CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN	PnIE.x	PnIFG.x	PnIES.x
P2Sel.3	P2DIR.3	P2DIR.3	P2OUT.3	Out1 signal†	P2IN.3	unused	P2IE.3	P2IFG.3	P2IES.3
P2Sel.4	P2DIR.4	P2DIR.4	P2OUT.4	Out2 signal†	P2IN.4	unused	P2IE.4	P2IFG.4	P2IES.4

† Signal from Timer_A

input/output schematic (continued)

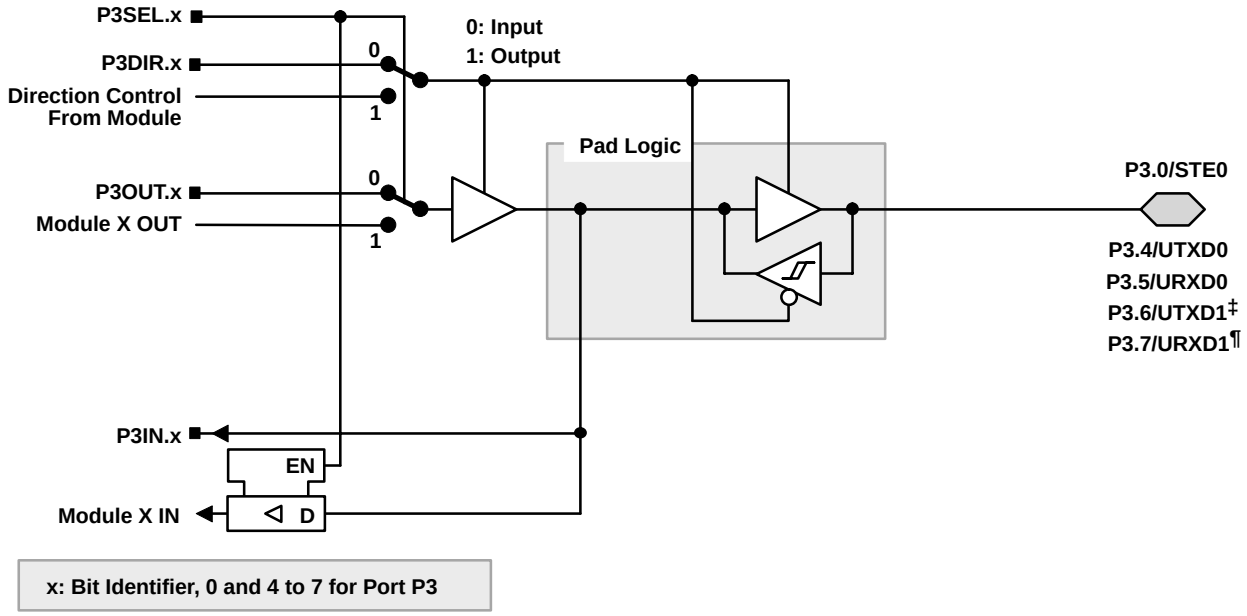
port P2, P2.5, input/output with Schmitt-trigger and R_{OSC} function for the basic clock module



PnSel.x	PnDIR.x	DIRECTION CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN	PnIE.x	PnIFG.x	PnIES.x
P2Sel.5	P2DIR.5	P2DIR.5	P2OUT.5	DV_{SS}	P2IN.5	unused	P2IE.5	P2IFG.5	P2IES.5

input/output schematic (continued)

port P3, P3.0 and P3.4 to P3.7, input/output with Schmitt-trigger

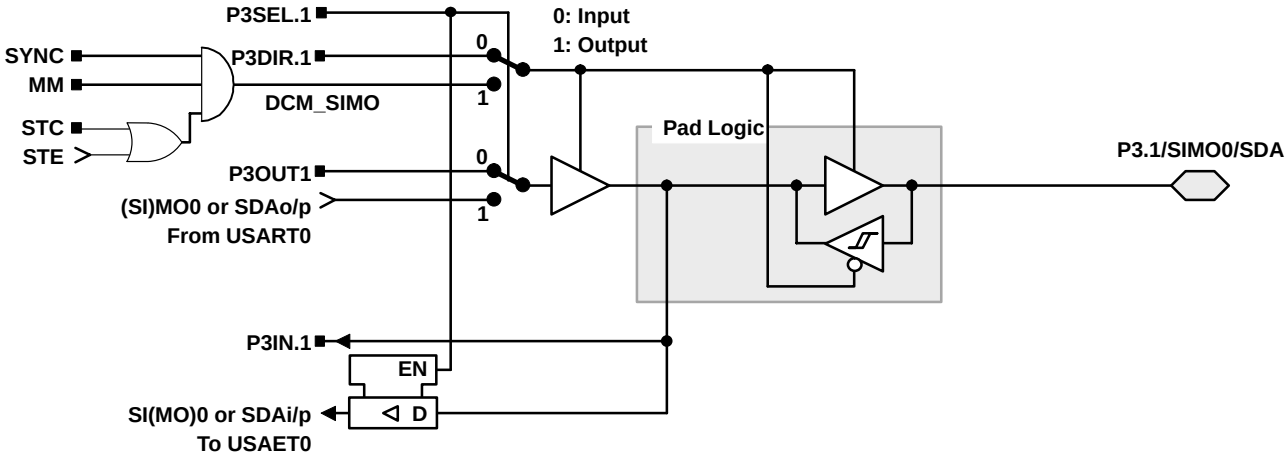


x: Bit Identifier, 0 and 4 to 7 for Port P3

PnSel.x	PnDIR.x	DIRECTION CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN
P3Sel.0	P3DIR.0	DV_{SS}	P3OUT.0	DV_{SS}	P3IN.0	STE0
P3Sel.4	P3DIR.4	DV_{CC}	P3OUT.4	UTXD0†	P3IN.4	Unused
P3Sel.5	P3DIR.5	DV_{SS}	P3OUT.5	DV_{SS}	P3IN.5	URXD0§
P3Sel.6	P3DIR.6	DV_{CC}	P3OUT.6	UTXD1‡	P3IN.6	Unused
P3Sel.7	P3DIR.7	DV_{SS}	P3OUT.7	DV_{SS}	P3IN.7	URXD1¶

† Output from USART0 module
‡ Output from USART1 module in x16x configuration, DV_{SS} in x15x configuration
§ Input to USART0 module
¶ Input to USART1 module in x16x configuration, unused in x15x configuration

port P3, P3.1, input/output with Schmitt-trigger



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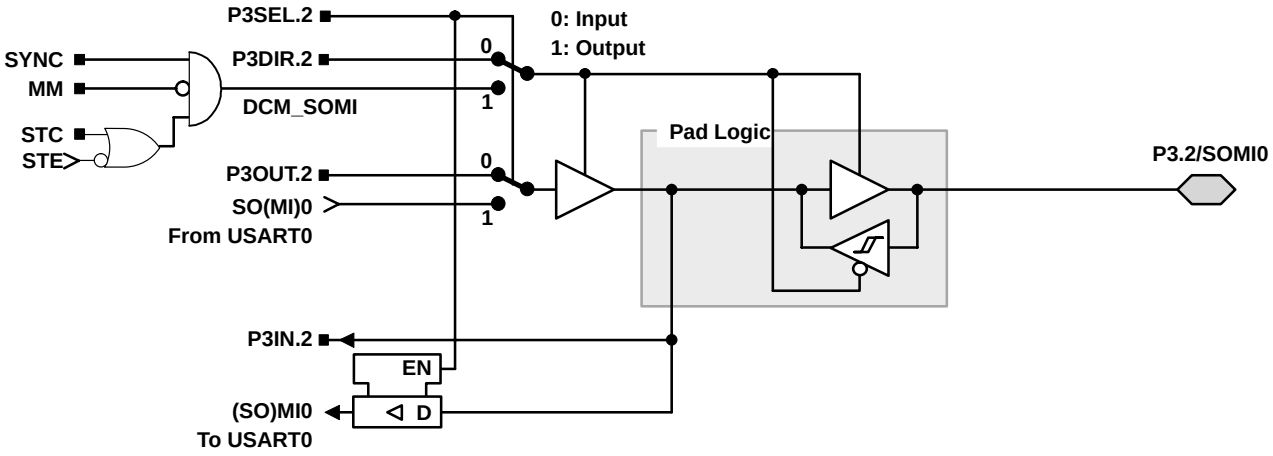
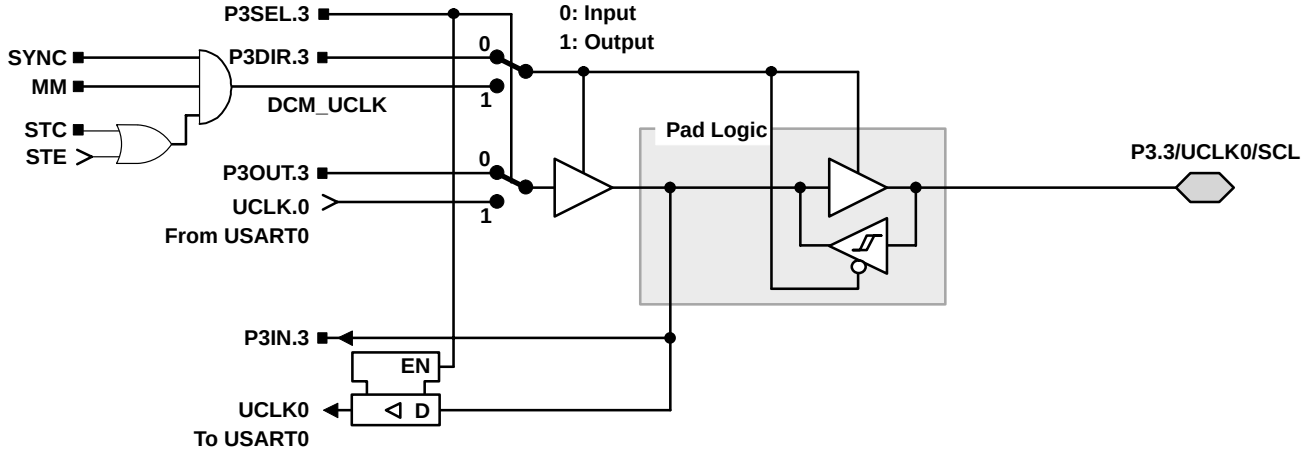
input/output schematic (continued)

port P3, P3.2, input/output with Schmitt-trigger



port P3, P3.3, input/output with Schmitt-trigger



NOTE: UART mode: The UART clock can only be an input. If UART mode and UART function are selected, the P3.3/UCLK0 is always an input.

SPI, slave mode: The clock applied to UCLK0 is used to shift data in and out.

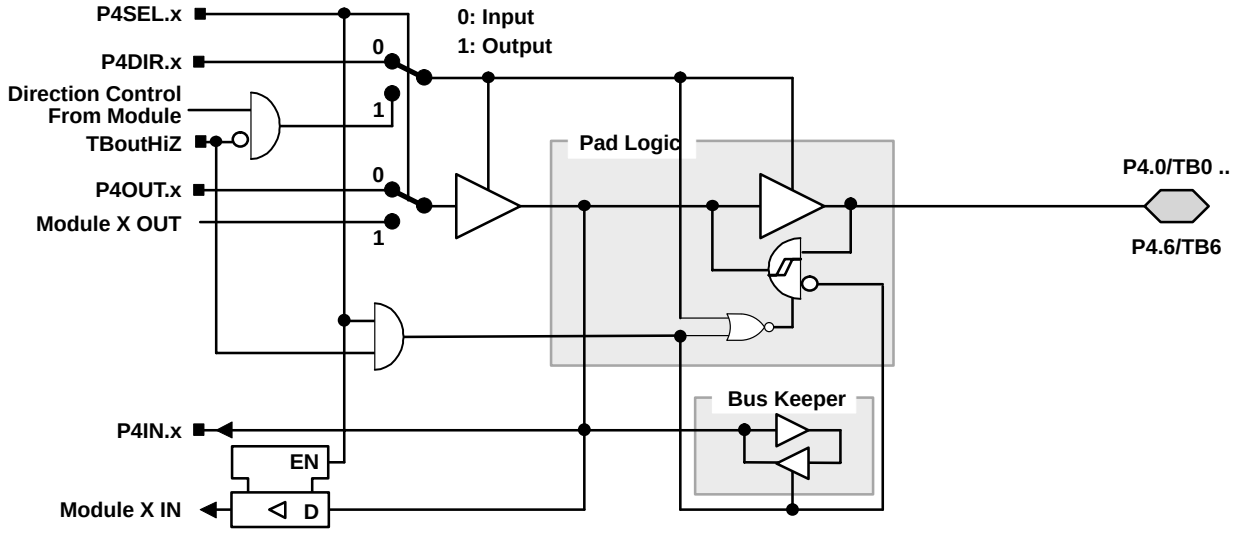
SPI, master mode: The clock to shift data in and out is supplied to connected devices on pin P3.3/UCLK0 (in slave mode).

I^2C, slave mode: The clock applied to SCL is used to shift data in and out. The frequency of the clock source of the module must be ≥ 10 times the frequency of the SCL clock.

I^2C, master mode: To shift data in and out, the clock is supplied via the SCL terminal to all I^2C slaves. The frequency of the clock source of the module must be ≥ 10 times the frequency of the SCL clock.

input/output schematic (continued)

port P4, P4.0 to P4.6, input/output with Schmitt-trigger



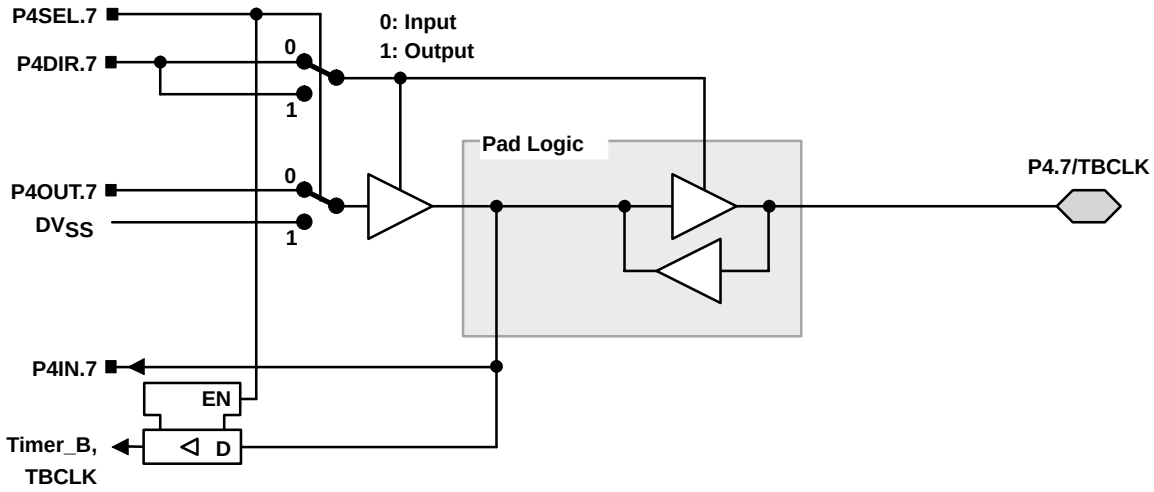
x: bit identifier, 0 to 6 for Port P4

PnSel.x	PnDIR.x	DIRECTION CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN
P4Sel.0	P4DIR.0	P4DIR.0	P4OUT.0	Out0 signal†	P4IN.0	CCI0A / CCI0B‡
P4Sel.1	P4DIR.1	P4DIR.1	P4OUT.1	Out1 signal†	P4IN.1	CCI1A / CCI1B‡
P4Sel.2	P4DIR.2	P4DIR.2	P4OUT.2	Out2 signal†	P4IN.2	CCI2A / CCI2B‡
P4Sel.3	P4DIR.3	P4DIR.3	P4OUT.3	Out3 signal†	P4IN.3	CCI3A / CCI3B‡
P4Sel.4	P4DIR.4	P4DIR.4	P4OUT.4	Out4 signal†	P4IN.4	CCI4A / CCI4B‡
P4Sel.5	P4DIR.5	P4DIR.5	P4OUT.5	Out5 signal†	P4IN.5	CCI5A / CCI5B‡
P4Sel.6	P4DIR.6	P4DIR.6	P4OUT.6	Out6 signal†	P4IN.6	CCI6A / CCI6B‡

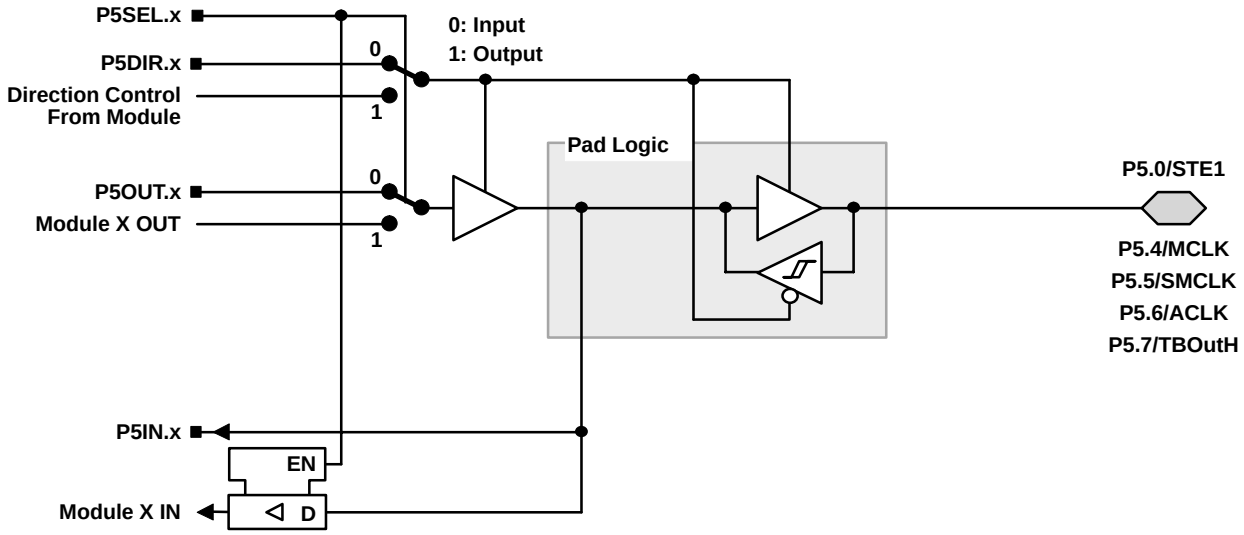
† Signal from Timer_B
‡ Signal to Timer_B

input/output schematic (continued)

port P4, P4.7, input/output with Schmitt-trigger



port P5, P5.0 and P5.4 to P5.7, input/output with Schmitt-trigger



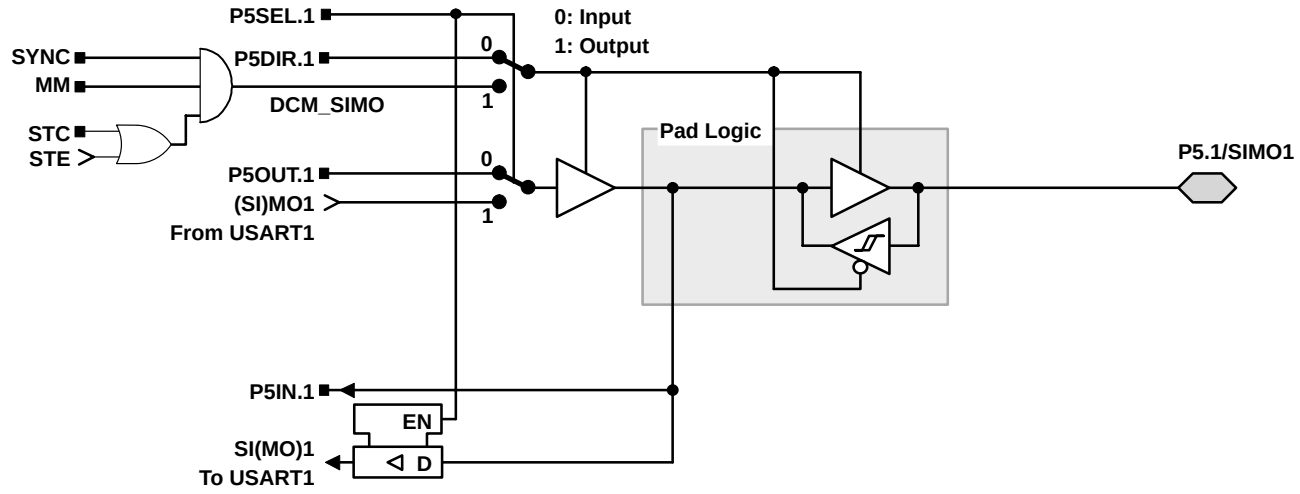
x: Bit Identifier, 0 and 4 to 7 for Port P5

PnSel.x	PnDIR.x	Dir. CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN
P5Sel.0	P5DIR.0	DV_{SS}	P5OUT.0	DV_{SS}	P5IN.0	STE.1
P5Sel.4	P5DIR.4	DV_{CC}	P5OUT.4	MCLK	P5IN.4	unused
P5Sel.5	P5DIR.5	DV_{CC}	P5OUT.5	SMCLK	P5IN.5	unused
P5Sel.6	P5DIR.6	DV_{CC}	P5OUT.6	ACLK	P5IN.6	unused
P5Sel.7	P5DIR.7	DV_{SS}	P5OUT.7	DV_{SS}	P5IN.7	TBoutHiZ

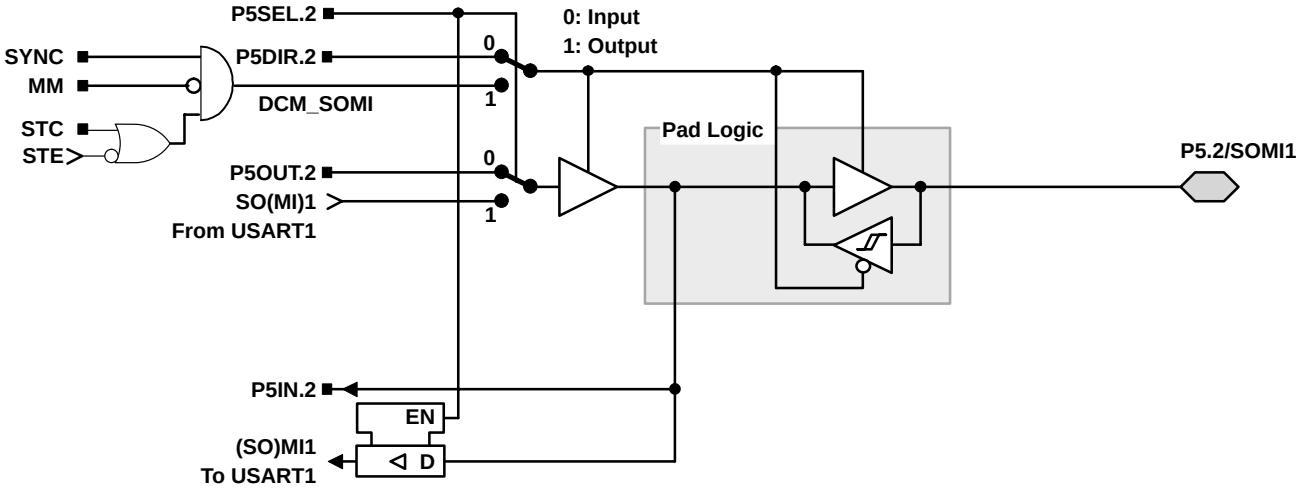
NOTE: TBoutHiZ signal is used by port module P4, pins P4.0 to P4.6. The function of TboutHiZ is mainly useful when used with Timer_B7.

input/output schematic (continued)

port P5, P5.1, input/output with Schmitt-trigger



port P5, P5.2, input/output with Schmitt-trigger



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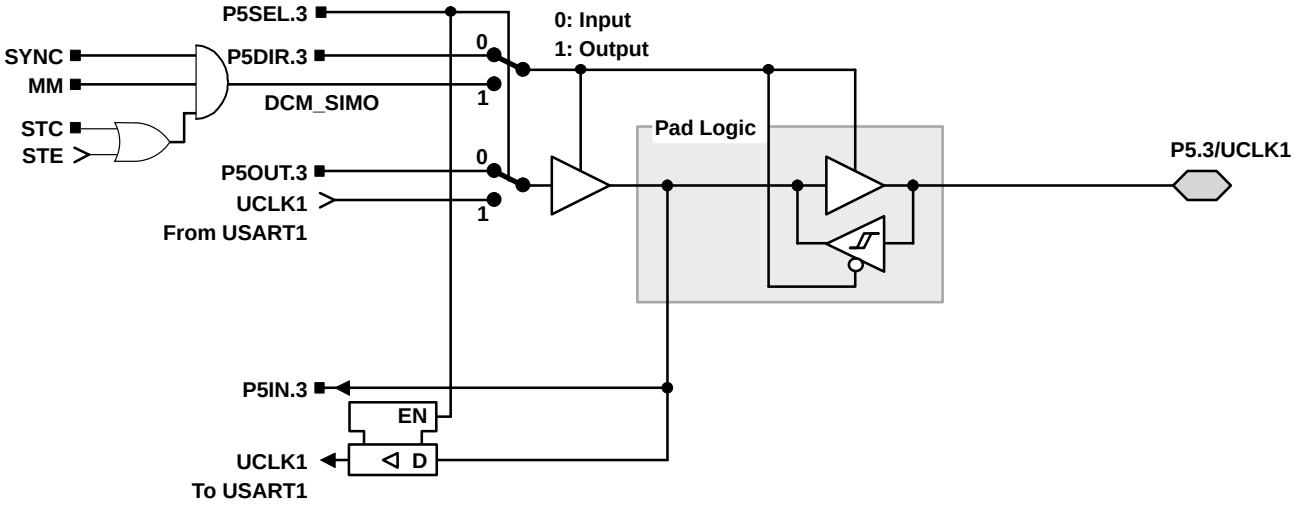
input/output schematic (continued)

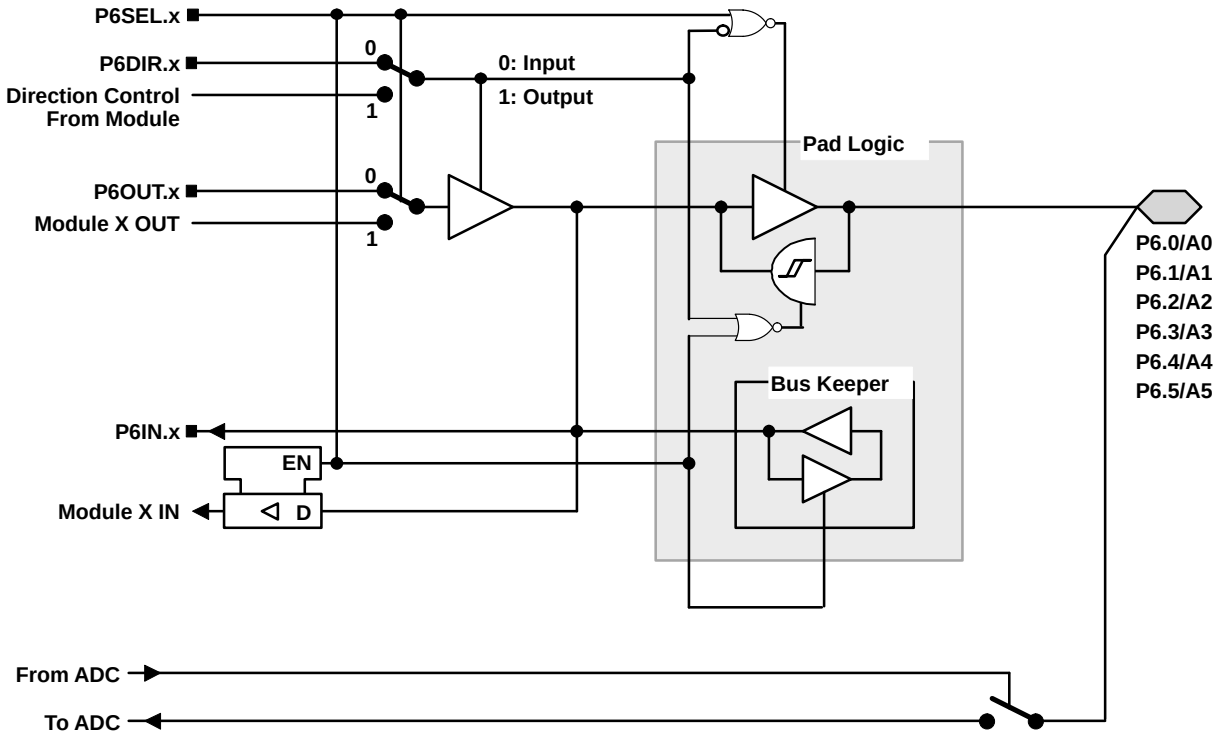
port P5, P5.3, input/output with Schmitt-trigger



NOTE: UART mode: The UART clock can only be an input. If UART mode and UART function are selected, the P5.3/UCLK1 direction is always input.
SPI, slave mode: The clock applied to UCLK1 is used to shift data in and out.
SPI, master mode: The clock to shift data in and out is supplied to connected devices on pin P5.3/UCLK1 (in slave mode).

input/output schematic (continued)

port P6, P6.0 to P6.5, input/output with Schmitt-trigger



x: Bit Identifier, 0 to 5 for Port P6

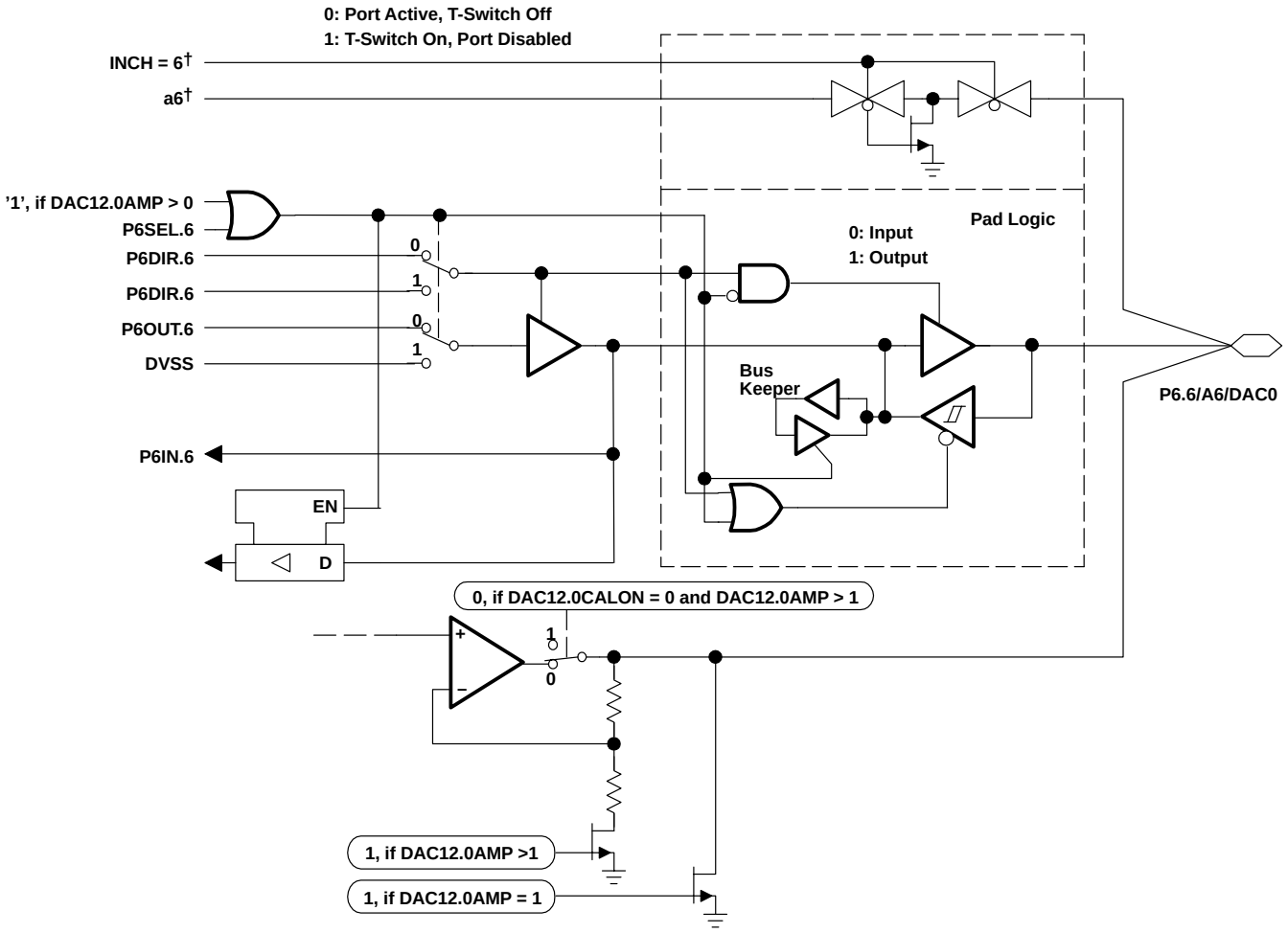
NOTE: Analog signals applied to digital gates can cause current flow from the positive to the negative terminal. The throughput current flows if the analog signal is in the range of transitions 0→1 or 1←0. The value of the throughput current depends on the driving capability of the gate. For MSP430, it is approximately 100 μA.
Use P6SEL.x=1 to prevent throughput current. P6SEL.x should be set, even if the signal at the pin is not being used by the ADC12.

PnSel.x	PnDIR.x	DIR. CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN
P6Sel.0	P6DIR.0	P6DIR.0	P6OUT.0	DV_{SS}	P6IN.0	unused
P6Sel.1	P6DIR.1	P6DIR.1	P6OUT.1	DV_{SS}	P6IN.1	unused
P6Sel.2	P6DIR.2	P6DIR.2	P6OUT.2	DV_{SS}	P6IN.2	unused
P6Sel.3	P6DIR.3	P6DIR.3	P6OUT.3	DV_{SS}	P6IN.3	unused
P6Sel.4	P6DIR.4	P6DIR.4	P6OUT.4	DV_{SS}	P6IN.4	unused
P6Sel.5	P6DIR.5	P6DIR.5	P6OUT.5	DV_{SS}	P6IN.5	unused

NOTE: The signal at pins P6.x/Ax is used by the 12-bit ADC module.

input/output schematic (continued)

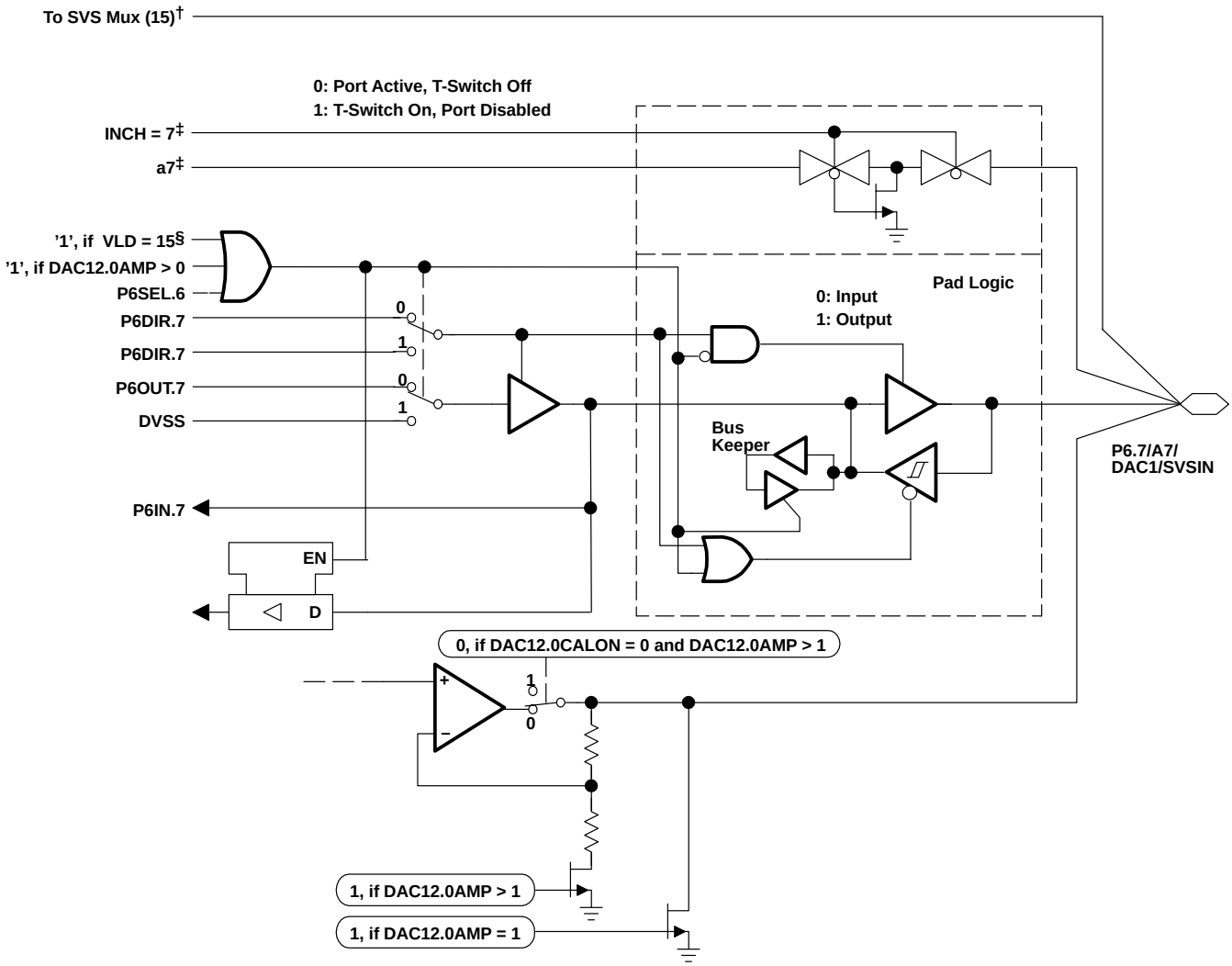
port P6, P6.6, input/output with Schmitt-trigger



†Signal from or to ADC12

input/output schematic (continued)

port P6, P6.7, input/output with Schmitt-trigger



†Signal to SVS Block, Selected if VLD = 15
‡Signal From or To ADC12
§VLD Control Bits are Located in SVS

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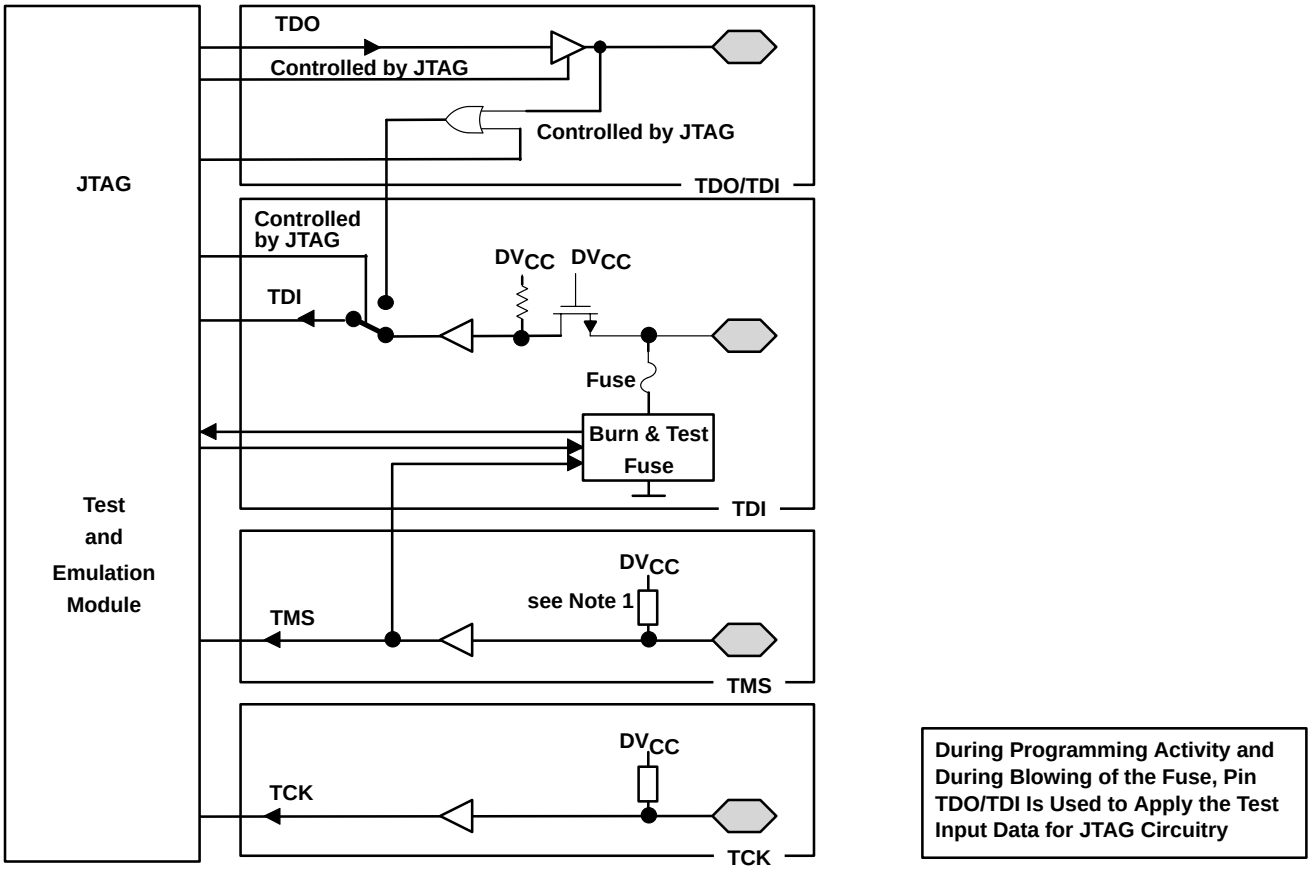
input/output schematic (continued)

JTAG pins TMS, TCK, TDI, TDO/TDI, input/output with Schmitt-trigger



JTAG fuse check mode

MSP430 devices that have the fuse on the TDI terminal have a fuse check mode that tests the continuity of the fuse the first time the JTAG port is accessed after a power-on reset (POR). When activated, a fuse check current, I_{TF}, of 1 mA at 3 V, 2.5 mA at 5 V can flow from the TDI pin to ground if the fuse is not burned. Care must be taken to avoid accidentally activating the fuse check mode and increasing overall system power consumption.

Activation of the fuse check mode occurs with the first negative edge on the TMS pin after power up or if the TMS is being held low during power up. The second positive edge on the TMS pin deactivates the fuse check mode. After deactivation, the fuse check mode remains inactive until another POR occurs. After each POR the fuse check mode has the potential to be activated.

The fuse check current will only flow when the fuse check mode is active and the TMS pin is in a low state (see Figure 18). Therefore, the additional current flow can be prevented by holding the TMS pin high (default condition).

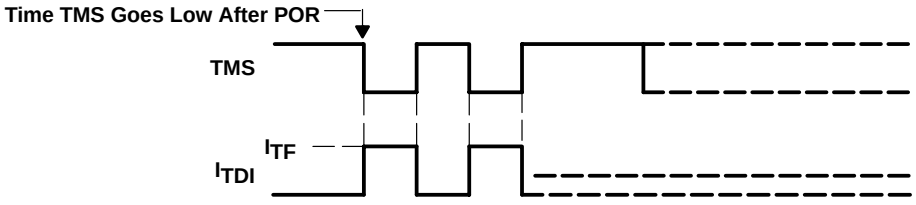
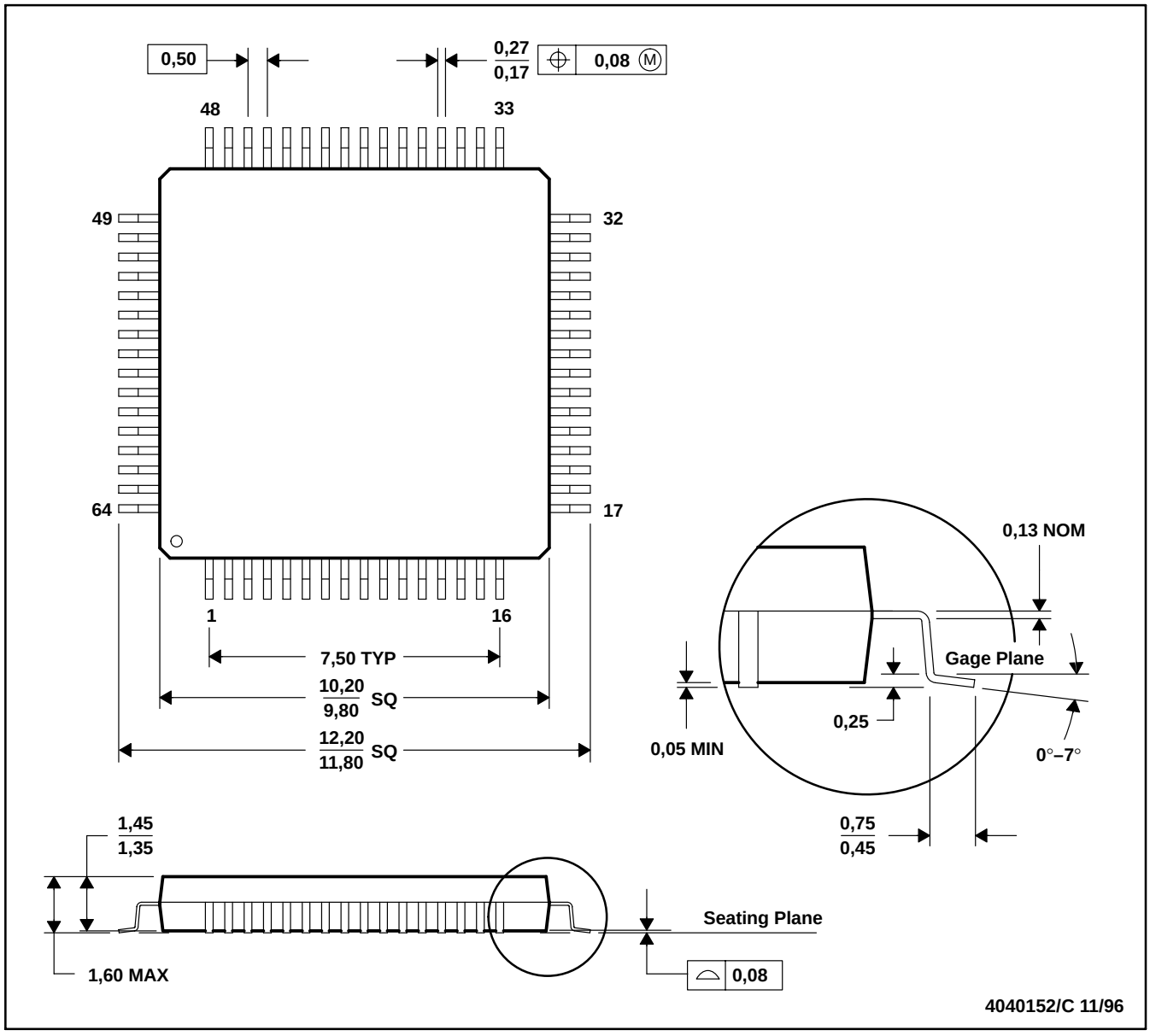


Figure 24. Fuse Check Mode Current, MSP430F15x, MSP430F16x

MECHANICAL DATA

PM (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026
D. May also be thermally enhanced plastic with leads connected to the die pads.

PRODUCT PREVIEW

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