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DESCRIPTION

The diags consist of board level and datapath tests. The individual tests in these sets are then organized into several “preset test sets”, which are the System Checks and Functional Tests. This procedure explains how to start TPS/ISE Board Level tests, what test LEDs are provided, where error messages are logged, and test descriptions. It applies to both 1.5T and 1.0T.

Note

Do not start multiple copies of diagnostics. Multiple copies of diagnostics can cause different anomalies such as locked up diagnostic windows.

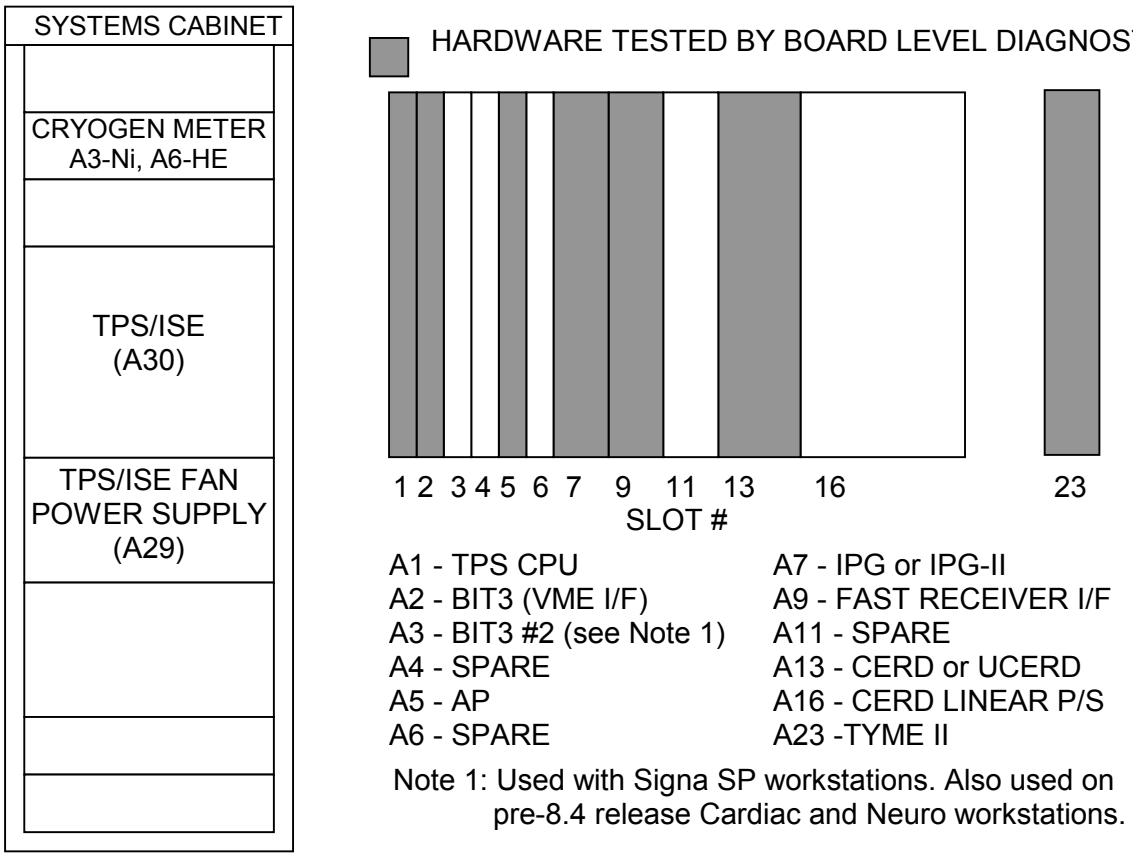
1- HARDWARE TESTED

Board level diagnostics (disk-based tests) check most of the TPS/ISE subsystem hardware. Refer to Table 1-1 for a list of tested boards; see Illustration 1-1 for the location of tested boards.

TABLE 1-1
HARDWARE TESTED

Hardware	Board Level Test?
CPU	No*
MEDCAM Board	Yes
VME I/F Board	Yes
Memory Board(s)	Yes
CERD or UCERD	Yes
IPG Board	Yes
TYME Board	Yes
Fast Receiver	Yes

*The CPU Board is tested by power-up diagnostics prior to the start of TPS/ISE Board Level tests.

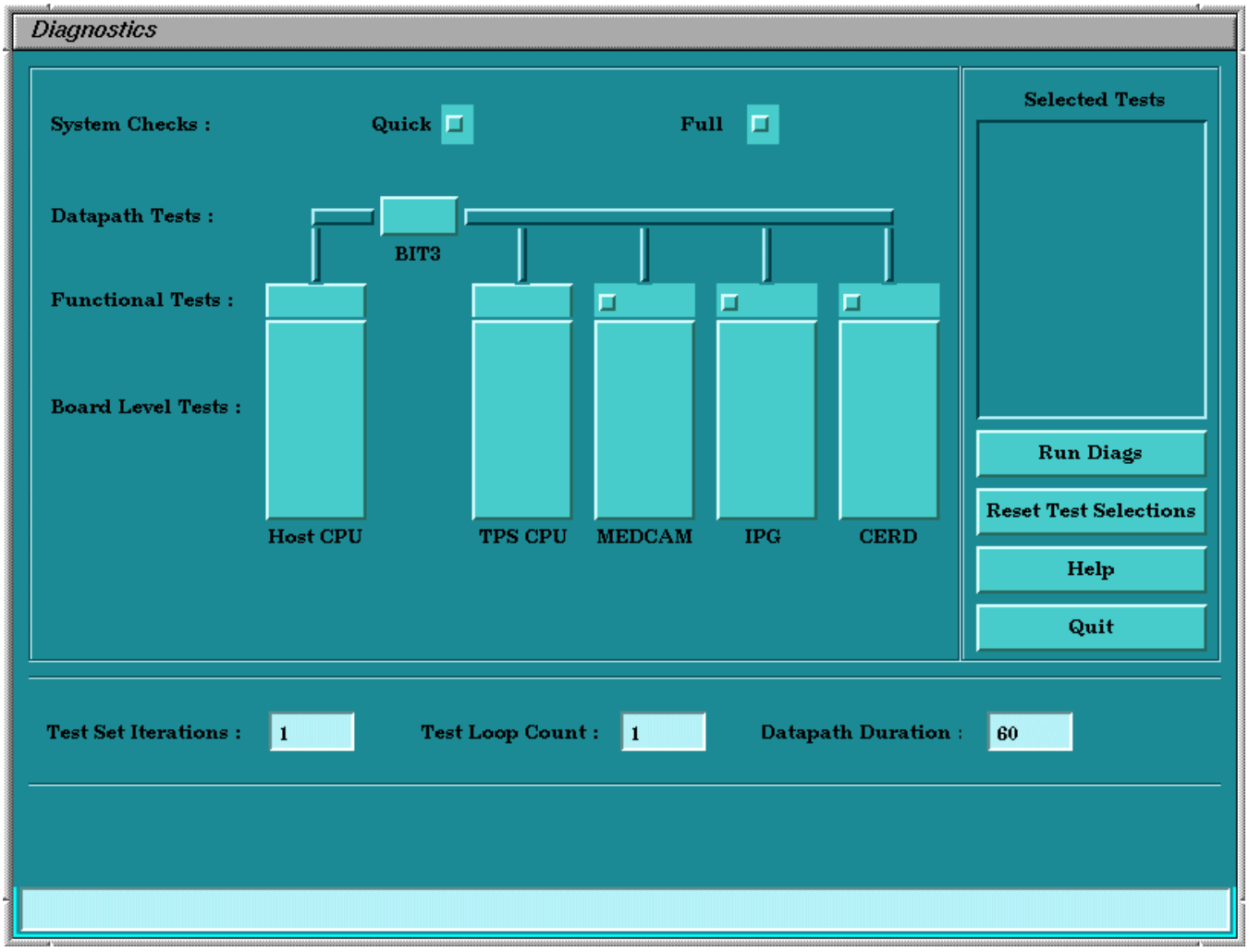


TPS/ISE TESTED HARDWARE LOCATION
ILLUSTRATION 1-1

2- STARTING TPS/ISE BOARD LEVEL TESTS

The board level tests are all disk-based and can be selected/run only when Signa 8.X software is running. These tests are downloaded to the TPS/ISE and run after the TPS/ISE EPROM-based tests have completed (refer to Procedure for TPS/ISE Power-Up Tests for EPROM-based test descriptions). Downloading is via the Bit 3 (TPS/ISE VME I/F) Board located in the TPS/ISE chassis. Status/error messages are returned to the Host computer for logging/display as applicable.

Board level tests may be initiated individually or in sets. Each procedure is described below. On the Service Desktop, select **[Diagnostics]**, **[Diagnostics Main Menu]**, then **[Start...]**. Wait for the Diagnostics Main Menu to appear. See Illustration 2-1.



DIAGNOSTICS MAIN MENU
ILLUSTRATION 2-1

The main diagnostics window consists of the following:

- The test selection area
- The selected tests area status window
- The function buttons:
  - **[Run Diags]** - Begins execution of the selected tests
  - **[Reset Test Selections]** - Clears all current test selections
  - **[Help]** - Displays a help file
  - **[Quit]** - Closes the diags menu
- Test control and information window
  - Test Iterations (**Note 1)** – The number of times the entire set of tests will run.
  - Loop count (**Note 1)** - The number of times each test will run.
  - Datapath duration (**Note 1)** - The number of seconds the datapath test(s) will run (only applies if datapath tests are selected).
  - Text information window - Test messages are displayed in this box.

Note 1: *This proprietary feature is available for GE use, and to sites with a valid Advanced Service Package Limited License.*

2-1 System Checks

Note

These diagnostic selections (see Illustration 2-1) are only displayed if a Service Key is installed. Refer to System Quick Check procedure. *This proprietary diagnostic/procedure is available for GE use, and to sites with a valid Advanced Service Package Limited License.*

2-2 DataPath Tests

The DataPath tests emphasize the backplane interconnections between the boards in the System Cabinet. Select DataPath test, and Datapath Duration (default test time is **60**), then select **[Run Diags]**. The data path tests run 60 seconds for one iteration count (loop). This allows all default tests to execute at least once. The data path test time may be changed later on the TPS/ISE Data Path Menu screen.

Note

The Bit 3 Data Path diagnostic button (beginning with Release 8.3; see Illustration 2-1) is only displayed if a Service Key is installed. Refer to procedure "Bit 3 Communication Troubleshooting". *This proprietary diagnostic/procedure is available for GE use, and to sites with a valid Advanced Service Package Limited License.*

2-3 Functional Tests

The Functional Tests are similar to the System Checks except that the tests are only targeted for the Medcam, CERD (or UCERD), and IPG Boards. As an example, the CERD Functional tests run all the CERD Board Level tests, and then only the Datapath tests involving the CERD automatically. It is intended to provide a fast method for suspected board failures and checking the functionality of the newly installed board in the system. Select Functional Tests, select MEDCAM, CERD, or IPG, then select **[Run Diags]**.

2-4 Board Level Tests

Select the appropriate board to be tested from the Diagnostic Main Menu. Wait for the submenu of the selected board to appear. A detailed description of each of the submenus begins in Section 4.

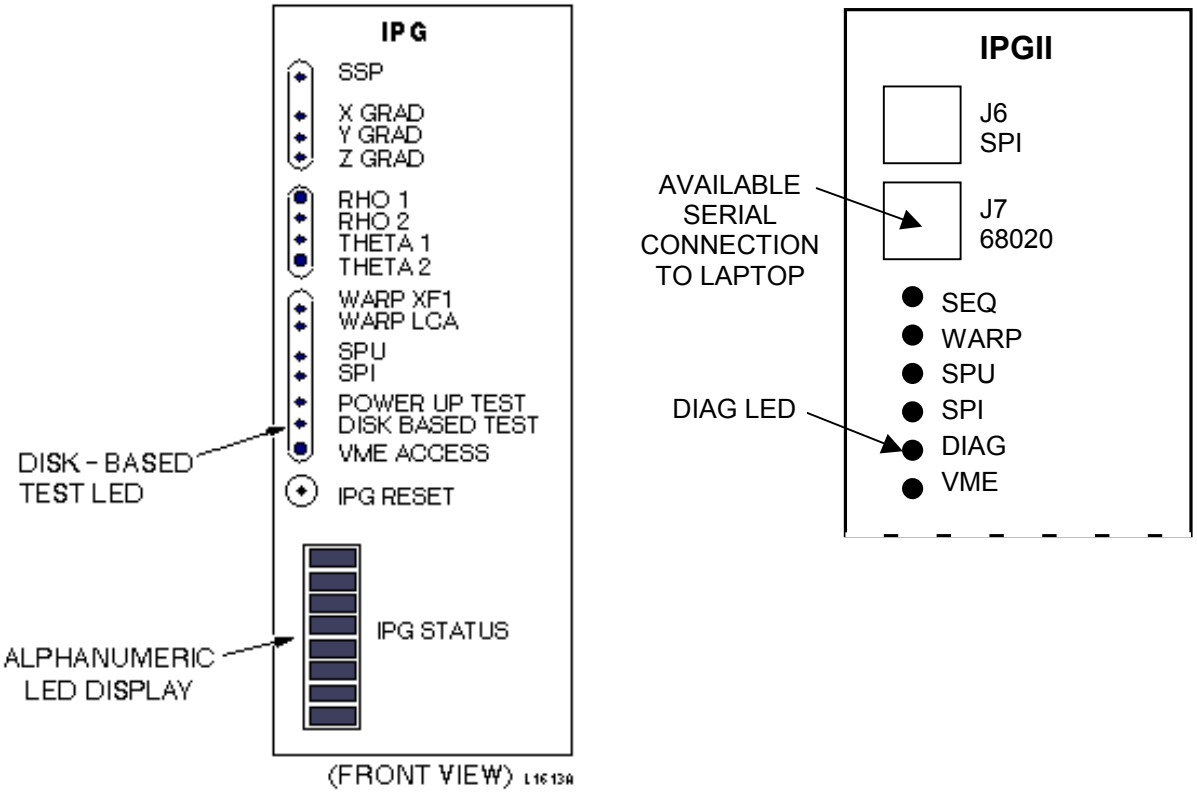
Select or deselect tests by clicking on the box that corresponds to the test(s) to be run. After all tests are selected, select Test Set Iterations (default is **1**), Test Loop Count (default is **1**), then select **[Run Diags]** from the Diagnostic Main Menu.

3- TPS/ISE TEST INDICATORS

3-1 Local Test Indicators

IPG: Local test indicators are provided on the TPS/ISE Integrated Pulse Generator (IPG) board. One green LED (DISK BASED TEST) and an alphanumeric display (IPG STATUS) provide the status of TPS/ISE disk-based tests and general subsystem activity. These LEDs (see Illustration 3-1) provide backup error/status indication for TPS/ISE tests in case communications with the host computer fails. While board level diagnostic tests are executing, the DISK BASED TEST LED lights. The IPG STATUS display also shows the abbreviated name of the test in progress.

IPG-II: One green LED (DIAG) and a serial connection (to laptop or PC) provides an indication of diagnostic tests (see Illustration 3-1). The LED and serial connection provide backup error/status indication for TPS/ISE tests in case communications with the host computer fails. (Refer to “TPS/ISE Serial Debug Connection”; *this proprietary procedure is available for GE use, and to sites with a valid Advanced Service Package Limited License.*)



LOCATION OF IPG TEST INDICATORS
ILLUSTRATION 3-1

3-2 Desktop Test Status Display

At the bottom of the Diagnostic Main Menu, messages such as "`Resetting TPS/ISE/IPG`", "`Downloading <test name>`", "`<test name> Running`", and "`Diagnostics Completed`" help indicate diagnostic test status.

3-3 Message Log

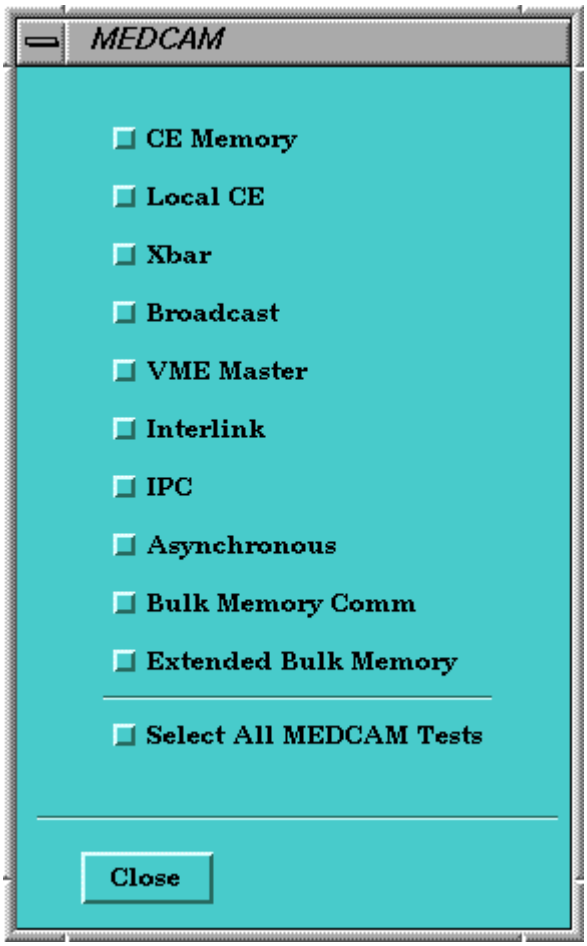
If an error occurs during board level tests, the error message(s) are reported to the Message Log. Be sure to set the viewing level to **[ALL]** to see diag error messages displayed in the Diagnostic Main Menu.

4- MEDCAM DIAGNOSTIC TEST DESCRIPTIONS

The Medcam board level diagnostics verify the functionality of the Memory Modules(s) and the Array Processor. The full set of tests requires the IPG, CERD, and CPU Boards.

4-1 MEDCAM Menu Test Descriptions

See Illustration 4-1 for MEDCAM Menu options and Table 4-1 for the test descriptions.



MEDCAM MENU OPTIONS
ILLUSTRATION 4-1

TABLE 4-1
MEDCAM TEST DESCRIPTIONS

TEST NAME	TEST DESCRIPTION
CE Memory	The Memory Tests check the CE data bus, address bus, and the byte, word, and double-word memory locations. The Memory Tests consist of a Basic Data Bus Test, a Data Pattern Test, a Byte Select Test, and a Byte Boundary Addressing Test.
Local CE Memory	The Local CE test phase is a comprehensive test of all of the hardware that is local to a particular CE. The Local CE Phase contains a Parity Test, FFT test, ECC Test, Interrupt Test, Timer Test, and FIFO Test. The description of these tests are as follows: The Parity Test checks the parity generating and checking hardware. The FFT Test stress-tests the MC860 board, using multiple passes of the FFT algorithm. After a given number of runs is completed, a value representing the total number of checksum failures is returned. A value of 0 indicates that the routine passed. The ECC Test verifies that the ECC circuitry in the CE ASIC can detect ECC errors for every bit and can generate interrupts. The Interrupt Test checks the functionality of the interrupt control circuitry, verifying that it can generate and clear interrupts. The Timer Test verifies that the timers in the CE ASIC can count down and generate interrupts. The FIFO Test checks the CE mailbox FIFO. It verifies that messages can be stored and read, the FIFO wraps, and interrupts can be generated and cleared.
Xbar	The i860 Xbar Test verifies the integrity of CE accesses through crossbars. The i860 writes and reads data patterns to CE memory through the crossbar ports and compares the data read with the data written.
Broadcast	The CE generates a broadcast command and verifies that the broadcast data is stored by all daughter cards (i.e., all bulk memory modules) installed.
VME Master	The VME Master tests the interaction of each CE with the host processor (TPS CPU) over the VME bus. In a single CE configuration, a VME target address is provided as a dmc argument, and the CE performs a variety of transfers to that buffer, which must be 64K long. Block and non-block DMAs of 8-, 16-, and 32-bit words are performed. The VME test also generates an interrupt at a specified vector and level on each loop of its execution.
Interlink	This test is valid only if more than one MEDCAM board is present. This test is not applicable to the GE MR system.
IPC	The Interprocessor Communication (IPC) Phase tests communications between CEs. Two or more CEs must be installed for this phase to execute. The IPC Phase contains the Lock test which executes locked cycles between CEs and verifies the integrity of the locked cycles.
Asynchronous	This test rigorously exercises crossbars and MEDCAM to MEDCAM VME interfaces, with all CEs executing simultaneously and accessing the memory of other CEs in a round-robin fashion. For our single CE system, this test is limited, with the CE performing worst-case timing tests of its own local memory.
Bulk Memory	Xbar communication from the CE to the daughterboard, (bulk memory modules) are tested.
Bulk Memory Walk	Xbar communication from the CE to the daughterboard, (bulk memory modules) are tested, as well as pattern, address and walking 1s/0s tests of each bulk memory module.

5- CERD DIAGNOSTIC TESTS

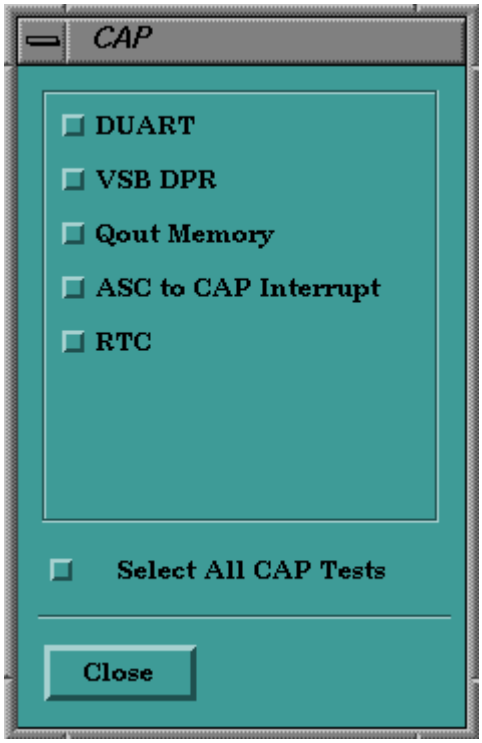
The Combined Exciter Receiver DAB (CERD) board level diagnostics verify the functionality of the entire CERD. The full set of tests requires the IPG, CPU, and AP.

5-1 CERD Menu Test Descriptions

The CERD Board Level Diagnostics can be separated into specific groups. See the Individual group for menu options (select the shadowed buttons for test descriptions).

5-1-1 CAP Menu Test Descriptions

See Illustration 5-1 for menu options. Refer to Table 5-1 for the test descriptions.



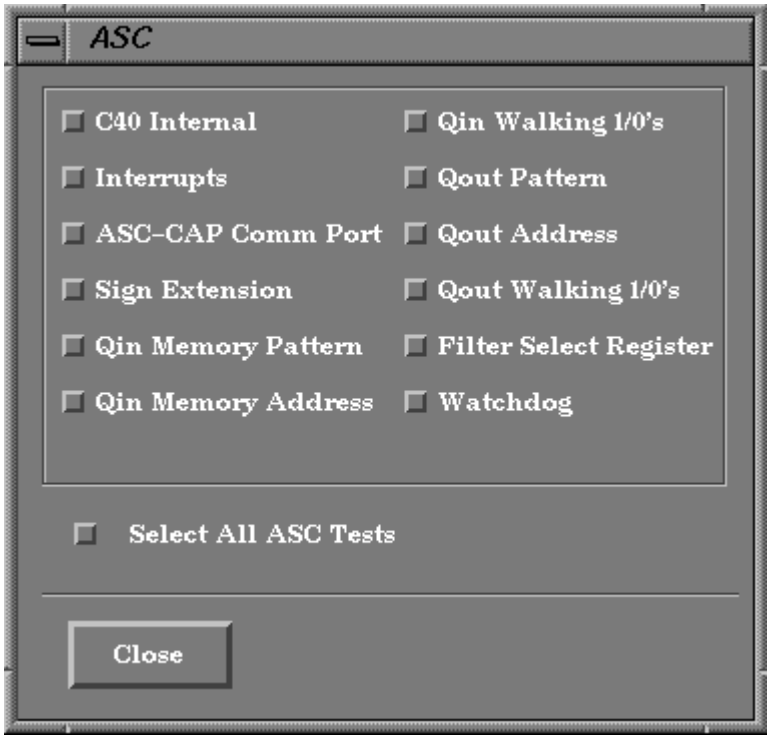
CAP MENU SELECTIONS
ILLUSTRATION 5-1

TABLE 5-1
CAP MENU TEST DESCRIPTIONS

TEST NAME	TEST DESCRIPTION
DUART	This test is run as one of the power up tests or as one of the CERD board level tests. DUART has two serial communication channels, ch.1 for debug terminal and ch.2 for RTC (Real Time Clock). This test does the local loop back tests on both channels.
VSB DPR	The VSB DPR test is a memory pattern and address test of the VSB DPR done from the CAP.
QOUT MEMORY	The AIME QOUT memory test uses the 24-bit memory test module.
ASC TO CAP INTERRUPT	The ASC to CAP Interrupt Test verifies the generation and reception of the interrupt from the ASC to the CAP.
RTC	

5-1-2 ASC Menu Test Descriptions

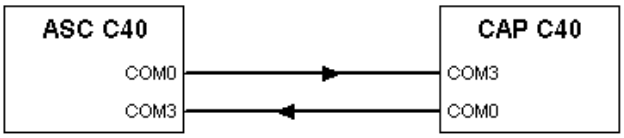
See Illustration 5-2 for menu options and Table 5-2 for test descriptions for the AIME "Scheduler And Controller."



ASC TEST MENU
ILLUSTRATION 5-2

TABLE 5-2
ASC TEST MENU DESCRIPTIONS

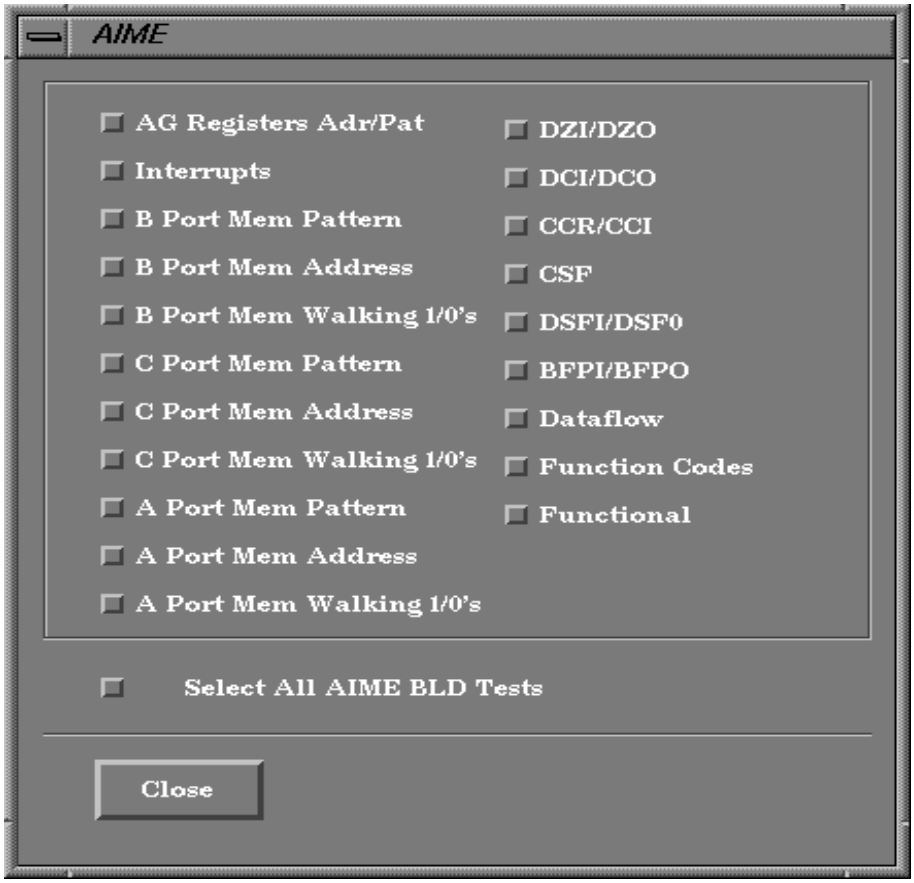
TEST NAME	TEST DESCRIPTION
C40 Internal	These tests verify many of the internal features of the TMS320C40 chip. They were written and provided (via a bulletin board service) by Texas Instruments, Inc. Please read the code and the related documentation for more information on these tests. Essentially, they stop when the first error is detected and they return a single error number. This number is added to an error message that is logged in the Genesis error data base. At the present time, the following C40 components/functions are tested. 1) Internal RAM 2) ARx Registers 3) Rx Registers 4) Status Register 5) Shifter 6) Multiplier 7) ALU 8) DMA 9) All instructions/addressing modes
Interrupts	This test verifies that the ASC recognizes and responds to all external interrupt sources. A list of ASC interrupt inputs and their sources is listed below. C40 SignalInterrupt Source IIOF0 AIME End of Pass Interrupt IIOF1 RAP Segment End Interrupt IIOF2 QIN/QOUT Bus Error Interrupt IIOF3 Filter Select Register Interrupt NMI Begin Acquisition Interrupt
ASC-CAP	The ASC and CAP communicate via a pair of C40 COMM ports as shown below. Each data path is tested as described below.

	 • Put all of the standard 32-bit data patterns into a server request packet and send it to the CAP. • After the CAP returns the packet, verify all of the data patterns. This test merely verifies that the comm port external connections are working properly. Clearly the comm port internal components are NOT exhaustively tested. This is done by the manufacturer. Plus, if the comm ports are not working correctly, the software will never get this far.
Sign Extension	Since QIN and QOUT memory are only 24-bits wide, the data in them must be sign extended to 32-bits when read back by the ASC. The sign extension hardware is tested as described below. • Enable ASC access to QIN and QOUT memory. • Write 0xFF7FFFFF to the first location in QIN memory (real component). • Read back the data and verify that it is equal to 0x007FFFFF due to the sign extension. • Write 0x00800000 to the first location in QIN memory. • Read back the data and verify that it is equal to 0xFF800000 due to the sign extension. Repeat the previous 4 steps using the first location of QOUT memory (real component).
Q_{in} Memory Pattern	QIN memory consists of two 32K x 24-bit memory banks: one bank stores the 24-bit real components of AIME data, and the other stores the 24-bit imaginary components. A standard 24-bit memory test is performed on each memory bank by the ASC. Since QIN memory can also be accessed by the RAP and the AIME, ASC access to QIN memory must be obtained prior to running this test. This is done using the appropriate utility routine: ax_setQINaccess (ASC_DEVICE).
Q_{in} Memory Address	An address pattern test is designed to verify that all memory locations are uniquely addressable (i.e., no address line shorts or address line open circuits exist). Beginning with a specified initial value, all memory is filled with an incrementing pattern. The entire pattern is read back and verified.
Q_{in} Walking 1/0's	A walking 1's and 0's test provides a more exhaustive check for shorts and open circuits among the memory data bits. <u>Walking 1's Test</u>: Using a start of value of 1, each memory location is loaded with the data value in the previous memory location shifted left by one bit. If the total number of shifts has exceeded the bit width of the memory, use the value 1 again. Continue filling memory this way until all memory has been filled. <u>Walking 0's Test</u>: Using a start of value of 0x7FFFFFFF, each memory location is loaded with the data value in the previous memory location shifted right by one bit. If the total number of shifts has exceeded the bit width of the memory, use the value 0x7FFFFFFF again. Continue filling memory this way until all memory has been filled.
Q_{out} Memory Pattern	A data pattern test consists of filling all memory with a constant data value and then reading back and verifying each memory location. This provides a simple (but not exhaustive) test of all data bits in the memory under test. In general, the following data patterns are used to check for data bit errors and any other forms of data pattern sensitivity in memory. The number and type of data patterns depends on the width of the memory under test.
Q_{out} Memory Address	An address pattern test is designed to verify that all memory locations are uniquely addressable (i.e., no address line shorts or address line open circuits exist). Beginning with a specified initial value, all memory is filled with an incrementing pattern. The entire pattern is read back and verified.
Q_{out} Walking 1/0's	A walking 1's and 0's test provides a more exhaustive check for shorts and open circuits among the memory data bits. <u>Walking 1's Test</u>: Using a start of value of 1, each memory location is loaded with the data value in the previous memory location shifted left by one bit. If the total number of shifts has exceeded the bit width of the memory, use the value 1 again. Continue filling memory this way until all memory has been filled.

	Walking 0's Test: Using a start of value of 0x7FFFFFFF, each memory location is loaded with the data value in the previous memory location shifted right by one bit. If the total number of shifts has exceeded the bit width of the memory, use the value 0x7FFFFFFF again. Continue filling memory this way until all memory has been filled.
Filter Select	An 8-bit address pattern test is performed on the Filter Select register. All possible 8-bit values (0 through 255) are written to this register by the CAP and read back and verified by the ASC. An external ASC interrupt is generated each time the CAP writes to the register; thus, the ASC reads and verifies the results in response to this interrupt. This test is implemented as described below. • Install an interrupt handler to catch the Filter select interrupt (IIOF3). • Construct a server request packet to write the value 0 to the Filter Select register and send this packet to the CAP for execution. • Start a 1-second timer. • Wait for the filter select interrupt to occur or the timer to expire. Report an error if the timer has expired; otherwise, continue with the test. • Stop the timer. • Read the filter select register and verify the data value. • Repeat the previous five steps for all data values 0 through 255 (you just did 0).
Watchdog	The ASC has a watchdog timer that will reset the ASC if the ASC ever fails to reset the timer for one second. The ASC resets the watchdog timer by toggling the TCLK0 pin once every second or faster. This test verifies that the watchdog timer is working and does reset the ASC if necessary.

5-1-3 AIME Menu Test Descriptions

See Illustration 5-3 for menu options and Table 5-3 for test descriptions for the "Advanced Integer Multiplier Engine."



AIME TEST MENU
ILLUSTRATION 5-3

TABLE 5-3
AIME TEST DESCRIPTIONS

TEST NAME	TEST DESCRIPTION
AG Register Adr/Pat	Each address generator (AG) contains 223 8-bit registers that are used to program the AG for a specific task. The data integrity of each register, the addressing of each register, and the correct and unique selection of each AG are exhaustively tested as follows. • Reset all of the AGs. • Perform a standard 8-bit data pattern test of all registers in an AG. Repeat the test for all five AGs. • Perform a standard 8-bit address pattern test of each AG register set. • Write a constant value to the first register of each AG, as shown below. AG #1 - Write 0x33 to the first 32 registers. AG #2 - Write 0x55 to the first 32 registers. AG #3 - Write 0xAA to the first 32 registers. AG #4 - Write 0xCC to the first 32 registers. AG #5 - Write 0xFF to the first 32 registers. Read back and verify the contents of each register. This test exposes any problems in AG chip selection that may exist.
Interrupts	The AIME generates an external ASC interrupt (IIOF0) at the end of each pass. The AIME End of Pass interrupt is tested as follows. • Load a simple program to move 256 data points from QIN memory to B port memory. The

	actual data values do not matter. • Start the AIME engine and wait (1 second) for the AIME End of Pass interrupt to occur. • Verify that the interrupt occurred. Report an error if the 1-second timer expired.
B Port Mem Pattern	The B port RAM that is connected to the LH9124 DSP chip must be tested by loading test data into QIN memory and then programming the AIME to write data to and read back data from B port RAM. Each pass of the memory test will be performed as described below. • Load QIN memory with the desired test pattern. Both the Real and Imaginary memory sections must be loaded. • Move the data from QIN memory to B port memory using the appropriate driver call. The driver call automatically programs and starts the AIME such that the data are transferred. • Move the data from B port memory to QOUT memory using the appropriate driver call. The driver call automatically programs and starts the AIME such that the data are transferred. • Verify the contents of QOUT memory and report any errors. The above procedure is repeated many times with a variety of data patterns.
B Port Mem Address	An address pattern test is designed to verify that all memory locations are uniquely addressable (i.e., no address line shorts or address line open circuits exist). Beginning with a specified initial value, all memory is filled with an incrementing pattern. The entire pattern is read back and verified.
B Port Mem Walking 1/0's	A walking 1's and 0's test provides a more exhaustive check for shorts and open circuits among the memory data bits. <u>Walking 1's Test</u> Using a start of value of 1, each memory location is loaded with the data value in the previous memory location shifted left by one bit. If the total number of shifts has exceeded the bit width of the memory, use the value 1 again. Continue filling memory this way until all memory has been filled. <u>Walking 0's Test</u> Using a start of value of 0x7FFFFFFF, each memory location is loaded with the data value in the previous memory location shifted right by one bit. If the total number of shifts has exceeded the bit width of the memory, use the value 0x7FFFFFFF again. Continue filling memory this way until all memory has been filled.
C Port Mem Pattern	This test is identical to the B port RAM test except that C port RAM is being tested.
C Port Mem Address	An address pattern test is designed to verify that all memory locations are uniquely addressable (i.e., no address line shorts or address line open circuits exist). Beginning with a specified initial value, all memory is filled with an incrementing pattern. The entire pattern is read back and verified.
C Port Mem Walking 1/0's	A walking 1's and 0's test provides a more exhaustive check for shorts and open circuits among the memory data bits. <u>Walking 1's Test</u> Using a start of value of 1, each memory location is loaded with the data value in the previous memory location shifted left by one bit. If the total number of shifts has exceeded the bit width of the memory, use the value 1 again. Continue filling memory this way until all memory has been filled. <u>Walking 0's Test</u> Using a start of value of 0x7FFFFFFF, each memory location is loaded with the data value in the previous memory location shifted right by one bit. If the total number of shifts has exceeded the bit width of the memory, use the value 0x7FFFFFFF again. Continue filling memory this way until all memory has been filled.
A Port Mem Pattern	This test is identical to the B port RAM test except that A port RAM is being tested; however, there is one unique aspect to this test that is NOT found in the B and C port RAM tests. The A port RAM consists of two 32K memory banks (bank 0 and bank 1). Bank 0 is a contiguous 32K memory bank while bank 1 can be configured as one contiguous 32K memory bank, as two 16K memory pages, or as four 8K memory pages. For this test, bank 1 will be configured as a contiguous 32K memory bank; the bank and page select mechanisms will be tested later on. Clearly, each 32K memory bank must be tested separately using the same procedure as described for the B port RAM test. The appropriate driver calls are used to make the desired memory bank and memory page selections throughout the execution of this test.
A Port Mem Address	An address pattern test is designed to verify that all memory locations are uniquely addressable (i.e., no address line shorts or address line open circuits exist). Beginning with a specified initial value, all memory is filled with an incrementing pattern. The entire pattern is read back and verified.
A Port Mem Walking1/0's	A walking 1's and 0's test provides a more exhaustive check for shorts and open circuits among the memory data bits.

	Walking 1's Test Using a start of value of 1, each memory location is loaded with the data value in the previous memory location shifted left by one bit. If the total number of shifts has exceeded the bit width of the memory, use the value 1 again. Continue filling memory this way until all memory has been filled. Walking 0's Test Using a start of value of 0x7FFFFFFF, each memory location is loaded with the data value in the previous memory location shifted right by one bit. If the total number of shifts has exceeded the bit width of the memory, use the value 0x7FFFFFFF again. Continue filling memory this way until all memory has been filled.
DZI/DZO	The DZI and DZO input pins of the LH9124 are used to "zero" data as it enters or leaves the LH9124 respectively. The DZI pin is controlled by the PO pin of the QIN AG while the DZO pin is controlled by the PO pin of the A port AG; thus, DZI and DZO are manipulated according to the address patterns generated by the QIN and A port AGs.
DCI/DCO	The DCI and DCO input pins of the LH9124 are used to complement/conjugate data as it enters or leaves the LH9124 respectively. The DCI and DCO pins are both controlled via the DSP Control Register.
CCR/CCI	The CCR and CCI input pins of the LH9124 are used to complement the real and imaginary components of coefficient (C port) data as it enters the LH9124. The CCR pin is controlled via the DSP Control Register. The CCI pin is controlled by the PO pin of the C port AG; thus, CCI is manipulated according to the address pattern generated by the C port AG.
CSF	The CCR and CCI input pins of the LH9124 are used to complement the real and imaginary components of coefficient (C port) data as it enters the LH9124. The CCR pin is controlled via the DSP Control Register. The CCI pin is controlled by the PO pin of the C port AG; thus, CCI is manipulated according to the address pattern generated by the C port AG.
DSF/DSFO	The DSFI[2:0] input pins of the LH9124 are used to shift right the real and imaginary components of the input data from 0 to 7 bit positions (i.e., divide by 1 to 128) during any pass.
BFPI/BFPO	The LH9124 contains a block floating-point accumulator that reads the value of the BFPI[5:0] input pins, adds in the number of right shifts (if any) that occurred during the current pass, and outputs the new accumulator value to the BFPO [5:0] output pins. During normal operation, the BFPO pins are fed back and connected to the BFPI pins. The only exception is during the first pass; at the start of the first pass, a user-supplied value (usually ZERO) is input on the BFPI pins in order to initialize the accumulator.
DataFlow	During any pass of AIME processing, data are read from an input port and the results are written to an output port. The data flow during each pass is controlled by the DF [2:0] bits in the DSP Control Register. The Dataflow test exercises each possible DF code such that any faulty data flow directions are easily detected.
Function Codes	The LH9124 can perform any one of 26 different functions during any pass. Correct operation of each function will be tested. They are summarized below. DSP / COMPLEX ARITHMETIC / VECTOR ARITHMETIC / VECTOR LOGICAL BWND 2CADD VADD VNAND BWND 4CSUB VSUB VNOR BRFT CMUL VMUL VXNOR BFCT CMAG VABS VPAS BFCT2 VMXM BCFIR BDFIR BRFIR Notice that there are actually only 21 function codes listed above. This is because the other five function codes are exhaustively tested elsewhere. Specifically, the MOVD and MOVC functions are used extensively by nearly all of the tests. Also, the radix butterfly function codes (BFLY2, BFLY4, and BFLY16) are thoroughly tested by the AIME Functional Tests.
Functional	This test performs a 256-point FFT on several input vectors and verifies the results of each. All input vectors are generated internally by the ASC. The expected results are stored internal to the test program. In some instances, the storage requirements are minimal due to the simple nature of the expected output vector; in other cases, a full 256-point complex output vector must be stored. All expected output vectors will be determined experimentally. They will also be verified using the SHARP Evaluation Module board set and again with the SHARP software simulator. Some of the output vectors (i.e., resulting from impulse and DC value input vectors) can also be determined mathematically for additional verification.

5-1-4 RAP Menu Test Descriptions

See Illustration 5-4 for menu options (select the shadowed buttons for test descriptions) for the "Raw Acquisition Processor."

RAP MENU SELECTIONS
ILLUSTRATION 5-4

TABLE 5-4
RAP MENU TEST DESCRIPTIONS

TEST NAME	TEST DESCRIPTION
Registers	Several of the RAP registers provide Read and Write access while others are Read Only. A standard data pattern and address test is performed on the registers that provide Read and Write access. Even though the address test is far from exhaustive, it is simple to do and does provide some useful test coverage.
Interrupts	Several of the RAP registers provide Read and Write access while others are Read Only. A standard data pattern and address test is performed on the registers that provide Read and Write access. Even though the address test is far from exhaustive, it is simple to do and does provide some useful test coverage.
FIFO Data	The RAP FIFOs are tested as described below. While the Data Pattern and Address tests verify the data and addressing integrity of the FIFOs, they cannot determine which FIFO is the actual cause of the error since there is no intermediate read back point between the Local XD FIFO and the Intra-RAP FIFO. A 16-bit data pattern test can be performed on all FIFO memory locations as follows. • Reset the entire RAP by setting the appropriate bits in the RAP Control Register. • Prevent RAP access to QIN memory (for now) by setting QIN access to the ASC. • Set the Receiver Select to EPI/Spectro mode, disable Feeder, and set the RAP Out Trigger Source to ASC_SOA. • Set the RAP Input and Output counters to 2048. • The ASC will now write 64 words of the current data pattern into the Local XD FIFO. Because the RAP has not been started yet, the data should "pile up" in the FIFO in order to test all FIFO memory locations. • Start the RAP by writing to the RAP Start Register.

<table>
<tr><td></td><td>• The ASC will now output 1984 (2048 - 64) additional data words into the Local XD FIFO. Since, data acquisition has started, all the Intra-RAP FIFO memory locations will become full. This tests all FIFO locations in the Intra-RAP FIFO.
• Enable RAP access to QIN memory. The RAP will now move all Intra-RAP FIFO data to QIN memory.
• The ASC will now verify all data in QIN memory.
•Repeat the previous steps for all other data patterns.</td></tr>
<tr><td>FIFO Address</td><td>This test is identical to the Data Pattern test as described in FIFO Data except that an address pattern is used as the test pattern.</td></tr>
<tr><td>XD FIFO Flags</td><td>The Local XD FIFO has a set of status flags that can be read by the CAP. These flags are tested as described below.

• Reset the entire RAP by setting the appropriate bits in the RAP Control Register.
• Send a request to the CAP to read the XD FIFO status flags.
• Verify the state of the status flags according to the following table. The state of the XD FIFO status flags depends on the number of words currently in the FIFO. Initially, the FIFO is empty.

<table>
<tr><th>Number of words in the XD FIFO</th><th>Almost Full/ Empty Flag</th><th>Half Full Flag</th></tr>
<tr><td>0 through 8</td><td>1</td><td>0</td></tr>
<tr><td>9 through 31</td><td>0</td><td>0</td></tr>
<tr><td>32 through 55</td><td>0</td><td>1</td></tr>
<tr><td>56 through 64</td><td>1</td><td>1</td></tr>
</table>
• Output 1 word (the actual value doesn't matter) to the Local XD FIFO.
•Repeat the previous three steps 63 more times. After the last iteration, the FIFO will be full.</td></tr>
<tr><td>Trigger Modes</td><td>The RAP Trigger Modes test verifies two of the three RAP Trigger modes: ASC SOA, and RAP Internal Triggering. The SSP SOA trigger mode is tested by the data path diagnostics. This test also checks the ability of the RAP to acquire a large segment of data and store it in QIN memory in smaller pieces (i.e., it tests the RAP retriggering ability).</td></tr>
<tr><td>Receiver Modes</td><td>The RAP Receiver Modes test verifies three receiver modes: single channel synchronous feeder, 4-channel synchronous feeder, and EPI/Spectro mode (asynchronous feeder). This test is performed as described below.

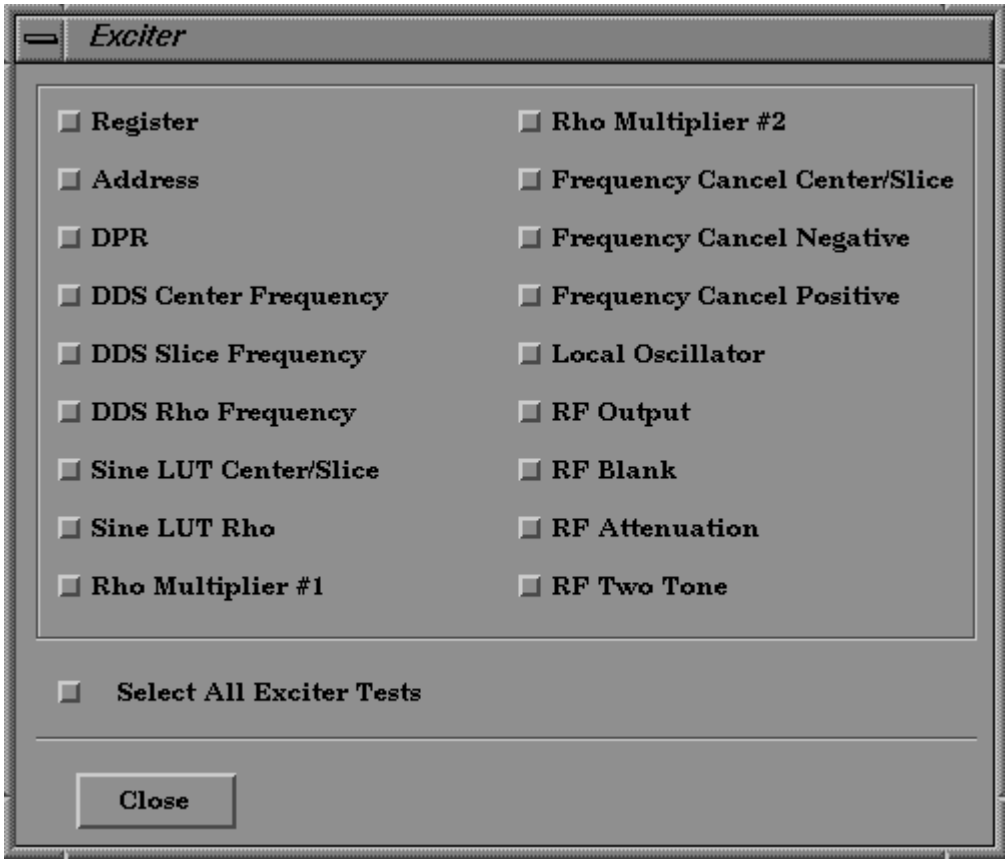
• Reset the entire RAP by setting the appropriate bits in the RAP Control Register.
• Set the Receiver Select to EPI/Spectro mode and disable Feeder.
• Set the RAP Out Trigger Source to ASC_SOA.
• Set the RAP Input and Output counters to 2048.
• Enable RAP access to QIN memory.
• Start feeding a 2048-point ramp data pattern to the Local XD FIFO. Start value = 0 and increment by 1 between each successive data point.
• Start the RAP by writing to the RAP Start Register.
• Wait for the RAP to finish. It generates a Segment End interrupt when done.
• Verify all data in QIN memory when done.
• Repeat the previous nine steps but this time set the Receiver Select to Single ARM mode, enable feeder, and increment the start value of the feeder ramp by 1.
•Repeat the nine steps again but this time set the Receiver Select to QUAD ARM mode, disable feeder, and increment the start value of the feeder ramp by 1. Also, only 512 data points need to be fed to the Local XD FIFO since each point will be sampled 4 times.</td></tr>
<tr><td>Offset</td><td>This test verifies the ability of the RAP to add an offset to each of the four receiver data paths.</td></tr>
<tr><td>Peak</td><td>The RAP Peak Detect Registers are tested using the following procedure.

• Reset the entire RAP by setting the appropriate bits in the RAP Control Register.
• Set the Receiver Select to QUAD ARM mode, enable Feeder, and set the RAP Out Trigger Source to ASC_SOA.
• Reset the Peak registers and reset the FIFOs.
• Set the RAP Input and Output counters to 16 (4 x 4).
• Enable RAP access to QIN memory.
• Feed the following four-point data sequence to the Local XD FIFO - 0x8001, 0, 0, 0.
• Start the RAP by writing to the RAP Start Register.
• Wait for the RAP to finish. It generates a Segment End interrupt when done.
• Read and verify the values in all four of the Peak registers.
• Repeat the previous seven steps using the following 4-point data sequence - 0, 0, 0, 0x8001. (i.e., put the non-zero data value at the end of the input sequence).
•Repeat the previous eight steps using a different non-zero input value. Increment this value by 1 for</td></tr>
</table>

	each iteration. (i.e., 0x8001, 0x8002, 0x8003, ..., 0xFFFE, 0xFFFF, 0x0000, 0x0001, 0x0002, ..., 0x7FFE, 0x7FFF).
Clip	The RAP Peak Detect Registers are tested using the following procedure. • Reset the entire RAP by setting the appropriate bits in the RAP Control Register. • Set the Receiver Select to QUAD ARM mode, enable Feeder, and set the RAP Out Trigger Source to ASC_SOA. • Reset the Peak registers and reset the FIFOs. • Set the RAP Input and Output counters to 16 (4 x 4). • Enable RAP access to QIN memory. • Feed the following four-point data sequence to the Local XD FIFO - 0x8001, 0, 0, 0. • Start the RAP by writing to the RAP Start Register. • Wait for the RAP to finish. It generates a Segment End interrupt when done. • Read and verify the values in all four of the Peak registers. • Repeat the previous seven steps using the following 4-point data sequence - 0, 0, 0, 0x8001. (i.e., put the non-zero data value at the end of the input sequence). •Repeat the previous eight steps using a different non-zero input value. Increment this value by 1 for each iteration. (i.e., 0x8001, 0x8002, 0x8003, ..., 0xFFFE, 0xFFFF, 0x0000, 0x0001, 0x0002, ..., 0x7FFE, 0x7FFF).
Overrange	This test verifies the ability of the RAP to detect overrange of post-offset corrected data in each of the four receiver data paths.
Demod	This test functionality checks the Disable Demodulation bit in the RAP Control register.

5-1-5 Exciter Menu Test Descriptions

See Illustration 5-5 for menu options and Table 5-5 for test descriptions for the Exciter portion of the CERD.



EXCITER TEST MENU
ILLUSTRATION 5-5

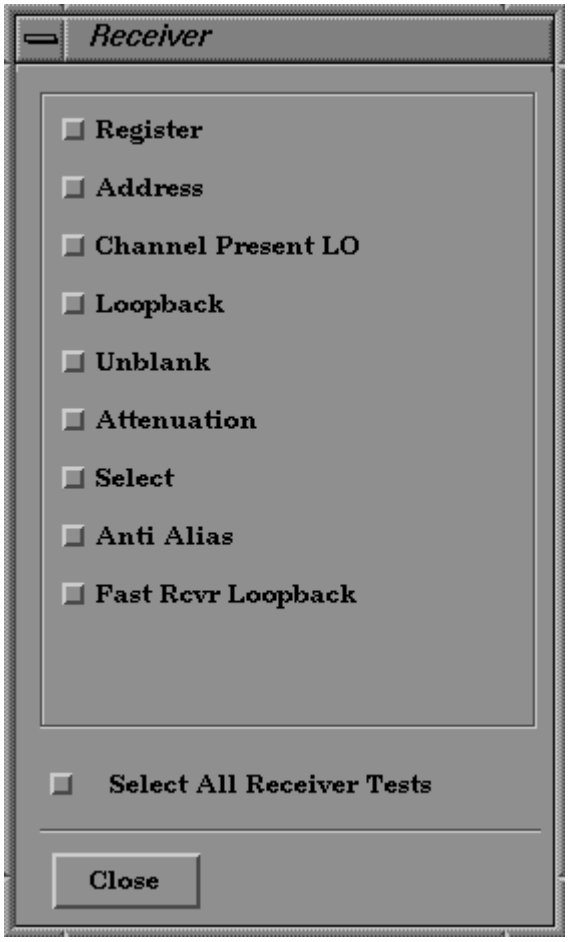
TABLE 5-5
EXCITER TEST DESCRIPTION

TEST NAME	TEST DESCRIPTION
Register	The following four 8-bit READ/WRITE registers of the Exciter are tested to ensure that data patterns written to them maintain their integrity when read back: 2x8-Bit Registers (HI and LO) 1. Transmit Atten Register 2. Theta Register 3. Rho Baseband Register 8-Bit Registers 4. Exciter Misc. CAP/SSP Register Failures can result from hardware failures in either input or readback latches.
Address	The following four 8-bit READ/WRITE registers of the Exciter are tested to ensure that data patterns written to them maintain their integrity when read back: 2x8-Bit Registers (HI and LO) 1. Transmit Atten Register 2. Theta Register 3. Rho Baseband Register 8-Bit Registers 4. Exciter Misc. CAP/SSP Register Failures can result from hardware failures in either input or readback latches.
DPR	The Exciter DPR memory test uses the 32-bit memory test module.

DDS Center Frequency	The Center DDS test verifies that the Direct Digital Synthesizers (DDS) are functioning properly. It does this by initializing the test path registers to zero, and then running the synthesizer input using the values 2x (where x = 13,14,...,23) until the output rolls over.
DDS Slice Frequency	The Slice DDS test verifies that the Direct Digital Synthesizers (DDS) are functioning properly. It does this by initializing the test path registers to zero, and then running the synthesizer input using the values 2x (where x = 13,14,...,23) until the output rolls over.
DDS Rho Frequency	The Rho DDS test verifies that the Direct Digital Synthesizers (DDS) are functioning properly. It will do this by initializing the test path registers to zero and then running the synthesizer input using the values 2x (where x = 13,14,...,23) until the output rolls over.
Sine LUT Center/Slice	The SINE LUT Center/Slice test clears all register and latch values that can reach the Sine LUT and writes input values to the Sine LUT via the THETA value register. This test then verifies that values written to the Sine LUT table produce correct output values.
Sine LUT Rho	This SINE LUT Rho test clears all register and latch values that can reach the Sine LUT and writes input values to the Sine LUT via the THETA value register. This test then verifies that values written to the Sine LUT table produce correct output values.
Rho Multiplier #1	The Rho Multiplier test verifies that this hardware multiplier is functioning properly. The test is divided into two separate tests to verify that both inputs of the hardware multiplier can be varied, and that they produce the correct output. For the first part of this test, the Rho DDS Phase and Frequency registers are initialized to produce an output of 1 at the Rho SINE LUT, which is input to the hardware multiplier. The other input of the multiplier is varied and the output of the multiplier is verified. For the second part of this test, initialize the Rho amplitude to have a value of 1, and vary the output of the SINE LUT via the Rho DDS Phase register. Check that the output of the hardware multiplier produces the correct corresponding sine values.
Rho Multiplier #2	The Rho Multiplier test verifies that this hardware multiplier is functioning properly. The test is divided into two separate tests to verify that both inputs of the hardware multiplier can be varied, and that they produce the correct output. For the first part of this test, the Rho DDS Phase and Frequency registers are initialized to produce an output of 1 at the Rho SINE LUT, which is input to the hardware multiplier. The other input of the multiplier is varied and the output of the multiplier is verified. For the second part of this test, initialize the Rho amplitude to have a value of 1, and vary the output of the SINE LUT via the Rho DDS Phase register. Check that the output of the hardware multiplier produces the correct corresponding sine values.
Frequency Cancel Center Slice	The Rho Multiplier test verifies that this hardware multiplier is functioning properly. The test is divided into two separate tests to verify that both inputs of the hardware multiplier can be varied, and that they produce the correct output. For the first part of this test, the Rho DDS Phase and Frequency registers are initialized to produce an output of 1 at the Rho SINE LUT, which is input to the hardware multiplier. The other input of the multiplier is varied and the output of the multiplier is verified. For the second part of this test, initialize the Rho amplitude to have a value of 1, and vary the output of the SINE LUT via the Rho DDS Phase register. Check that the output of the hardware multiplier produces the correct corresponding sine values.
Frequency Cancel Negative	The Center/offset (slice) Frequency Cancellation test verifies that the center and negative offset frequency DDSs cancel the effects of one another when given opposing frequencies.
Frequency Cancel Positive	The Center/offset (slice) Frequency Cancellation test verifies that the center and negative offset frequency DDSs cancel the effects of one another when given opposing frequencies.
Local Oscillator	The Center/offset (slice) Frequency Cancellation test verifies that the center and negative offset frequency DDSs cancel the effects of one another when given opposing frequencies.
RF Output	This test verifies that RF output level is correct for various settings of attenuation, Rho amplitude, and center frequency.
RF Blank	This test verifies that the RF blank attenuator has at least 60 dB of attenuation.
RF Attenuation	This test verifies the operation of the coarse and fine attenuators.
Two Tone	This test verifies the amplitude characteristics of the narrow band analog filter. Unlike the Narrowband Filter Select Test, which uses a sinc signal, this test exercises the filter with two specific frequencies. A RHO signal of 15.625 kHz is created by the CAP. This causes a two-tone signal to be transmitted at ±15.625 kHz of the base RF frequency. There are significant third-order intermodulation products at ±46.875 kHz produced during demodulation to 125 kHz. These products are within the passband of the anti-alias lowpass filter and outside the passband of the switchable narrowband prefilter.

5-1-6 Receiver Menu Test Descriptions

See Illustration 5-6 for the Receiver portion of the CERD menu. Refer to Table 5-6 for test descriptions.



RECEIVER TEST MENU
ILLUSTRATION 5-6

TABLE 5-6
RECEIVER TEST DESCRIPTIONS

TEST NAME	TEST DESCRIPTION
Register	The following four 8-bit READ/WRITE registers of the Receiver are tested to ensure that data patterns written to them maintain their integrity when read back: 2x8-Bit Registers (HI and LO) 1. Transmit Atten Register 2. THETA Register 3. RHO Baseband Register 8-Bit Registers 4. Receiver Misc. CAP/SSP Register Failures in these tests can result from hardware failures in either input or readback latches.
Address	The following four 8-bit READ/WRITE registers of the Receiver are tested to ensure that data patterns written to them maintain their integrity when read back: 2x8-Bit Registers (HI and LO) 1. Transmit Atten Register 2. THETA Register 3. RHO Baseband Register

	8-Bit Registers 4. Receiver Misc. CAP/SSP Register Failures in these tests can result from hardware failures in either input or readback latches.
Channel Present LO	The following four 8-bit READ/WRITE registers of the Receiver are tested to ensure that data patterns written to them maintain their integrity when read back: 2x8-Bit Registers (HI and LO) 1. Transmit Atten Register 2. THETA Register 3. RHO Baseband Register 8-Bit Registers 4. Receiver Misc. CAP/SSP Register Failures in these tests can result from hardware failures in either input or readback latches.
Loopback	This test verifies that the analog receiver modules can correctly receive a known signal from the Exciter. The Exciter is set up to use DC modulation and the ASC computes the received amplitude. Two different amplitudes are transmitted. The first amplitude is zero so the receiver should be getting only noise plus any offset variation. The second amplitude is 32752 at the Exciter and should be 29190 at the receiver (this checks net gain). This test assumes that the gain and offset of each receiver are not calibrated. A (±32 LSBs) offset tolerance is allowed for each receiver. A five percent total gain tolerance (±1460 LSBs) is allowed for each receiver. Noise must be within ±13 LSBs. The reference for noise is an averaged signal. The average signal is a crude compensation for gain and offset variations.
Unblank	This test checks that the RF blank attenuator works properly on each receiver module. When enabled, the RF blank attenuator should attenuate the received signal by 60 dB (0.001 amplitude).
Attenuation	This test verifies all sixteen possible R1 attenuation values on each receiver module. The ranges of acceptable amplitudes take into consideration the following hardware tolerances: The receiver input amplifier can vary by ±0.5 dB (±6%). The total ripple of all the receiver filters should be within ±0.5 dB (±6%). The R1 attenuator can vary by ±0.25 to 1.25 dB (±3 to 15%).
Select	This test verifies that each receiver module can be uniquely selected. All receiver modules are fed the same signal, but the R1 attenuation of each receiver is different, so the received amplitudes should be different. The ranges of acceptable amplitudes take into consideration the following hardware tolerances: The receiver input amplifier can vary by ±0.5 dB (±6%). The total ripple of all the receiver filters should be within ±0.5 dB (±6%). The R1 attenuator can vary by ±0.25 to 1.25 dB (±3 to 15%).
Anti Alias	This test verifies the frequency response of the ADC antialias filter within certain frequency ranges. It checks for 1.0 dB flatness within 62.5 to 187.5 kHz passband. Center frequency at 125 kHz is skipped because we get a mysterious dimple in the FFT at that frequency. Of the 1.0 dB flatness allowed, approximately 0.5 dB is due to the coarseness of the 8-bit RHO sinc signal.
Fast Rcvr Loopback	This test verifies the basic operation of all Fast Receiver components with emphasis on the analog signal path. First of all, the average DC offset in each of the Analog Module signal paths (i.e., I and Q) is computed and checked. These values are also used to offset-correct all data in the remainder of this test. Next, the overall analog gain is computed and checked. Finally, the overall RMS noise in the analog signal path is measured and verified. Note that this test is similar to the Loopback test that is part of the CERD Receiver diags.

6- IPG DIAGNOSTIC TESTS

The Integrated Pulse Generator (IPG) Serial Peripheral Interface (SPI)/ Signal Processing Unit (SPU)/ Waveform Rotation Processor (WARP) board level diagnostics verify the functionality of the IPG hardware accessed and controlled by the SPI, SPU, and/or WARP processors. The full set of tests requires the IPG, CPU, and AP Boards.

The Integrated Pulse Generator (IPG) Basic Board Level Diagnostics verify the functionality of the IPG hardware accessed and controlled by the IPG CPU. The full set of IPG tests requires the IPG, CPU, and AP Boards. IPG Board Level Diagnostics are separated into three groups.

6-1 IPG BLD Menu Test Descriptions

See Illustration 6-1 for IPG BLD (Board Level Diagnostics) Menu options and Table 6-1 for the test descriptions.

IPG BLD TEST MENU
ILLUSTRATION 6-1

TABLE 6-1
IPG BLD TEST DESCRIPTIONS

TEST NAME	TEST DESCRIPTION
SPU DPR	Test time is ~5 seconds. This test verifies the functionality of the entire range of SPU Dual Port RAM. The RAM is tested with a pattern test using 55555555, AAAAAAAA, 33333333, 0F0F0F0F, 00FF00FF, 0000FFFF and an address test which will write each DPR location's 32-bit addresses as data and then verify that each location contains its address. During these tests, the SPU is held "reset".
SPI DPR	Test time is ~5 seconds. This test verifies the functionality of the entire range of SPI Dual Port RAM. The RAM is tested with a pattern test using 5555, AAAA, 3333,0F0F, 00FF and an address test which will write each DPR location's 16-bit addresses as data and then verify that each location contains its address. During these tests, the SPU is held "reset".
WARP DPR	Test time is ~5 seconds. This test verifies the functionality of the entire range of WARP Dual Port RAM. The RAM is tested with a pattern test using 55555555, AAAAAAAA, 33333333, 0F0F0F0F, 00FF00FF, 0000FFFF and an address test which will write each DPR location's 32-bit addresses as data and then verify that each location contains its address. During these tests, the SPU is held "reset".
SPU Local	Test time is ~31 seconds. This set of tests verifies the functionality of the SPU processor. The SPU is downloaded with diagnostics code which is then executed under control of the IPG CPU. The following is a list of the tests included in this diagnostic set.: Internal RAM Test, Local SRAM Test, and SPU-SPI Dual Port RAM Test - Although these RAM exist in different locations, each of these tests use the same three subtests to verify RAM operation: a pattern test, an address test and a 1's/0's test. The pattern test uses 55555555, AAAAAAAA, 333333333, 0F0F0F0F, 00FF00FF, 0000FFFF patterns to verify that each bit in RAM can be set and reset. The address test uses 31-bit long word addresses which are written and checked to verify that the address lines are performing correctly. Finally, the sliding 1's/0's test verifies that proper setting and clearing of bits occurs, and that erroneous writes to blocks of memory do not occur. Refer to Section 1-4-2, Memory Menu Tests, Table 1-3 for more information about the sliding 1's/0's test. Interrupt Test - This test verifies the proper operation of the SPU CPU Interrupts. This test is composed of three checks: External Interrupt Check, Interrupt Disable Check, and Interrupt Generation Check. At the beginning of these tests, the Global Interrupt Enable (GIE) control bit, the Status Register and Interrupt Enable (IE) and Interrupt Flag (IF) Registers are all cleared. External Interrupt Check verifies that no external device is continuously generating interrupts. If the content of the IF Register is not zero after initialization, a failure occurs. The Interrupt Disable Check verifies that the GIE bit and IE Register disables all interrupts. If they do not, a failure occurs. The Interrupt Generation Check verifies that an internal interrupt can be generated and received properly. It also verifies that the interrupt cycle clears the IF bit, but not the GIE bit. Timer Test - This test verifies that the internal timers in the SPU CPU are operational. This test checks for the ability of the timers to count linearly and to provide interrupts to the CPU. DMA Test - This test verifies that the on-chip DMA controller is functioning properly. The DMA transfer occurs from one section of Processor RAM to another section of Processor RAM. This test contains three subtests: DMA Data Transfer Test, DMA Interrupt Test, and DMA Synchronization Test. • DMA Data Transfer Test verifies that all data can be transferred accurately. • DMA Interrupt Test verifies that a DMA Interrupt can be generated and received properly. • DMA Synchronization Test verifies that a data transfer can be synchronized with interrupts. Serial Port Test - This test verifies that the two serial ports from the processor are operating properly.
SPI Local	Test time is ~30 seconds. This set of tests verifies the functionality of the SPI processor. The SPI is downloaded with diagnostics code which is then executed under control of the IPG CPU. The following is a list of the tests included: Static RAM Test - This test verifies the operation of the Static RAM (SRAM). This test uses both

	pattern tests and address tests. The pattern tests include the following 8-bit and 16-bit patterns: (8-bit) 0x55, 0xAA, 0x33, and 0x0F; (16-bit) 0x5555, 0xAAAA, 0x3333, 0x0F0F, and 0x00FF. These patterns are used to verify that each bit in RAM can be set and reset. The address test writes and checks data in each address location to verify the address lines are performing correctly. Single Sided Dual Port RAM Test - This test verifies the functionality of the Dual Port RAM (DPR) from the SPI and IPG sides. It also verifies the integrity of both the DPR access and storage hardware from the SPI side. To do this, the test uses standard memory read/write tests. For the IPG-SPI DPR, 16-bit patterns and addresses are used, while for SPU-SPI DPR, 8-bit patterns and address patterns are used. SPU-SPI Dual Port RAM Interrupts/Synchronized Tests - This test verifies the proper operation of interrupt handlers between the SPU and SPI. These tests are identical to the above tests for the IPG-SPI DRAM Interrupts/Synchronized Tests, but use the SPU processor instead of the IPG processor. UART Test - This test verifies that DUART 1 Channel A (SRI interface), DUART 1 Channel B (GCP interface) and DUART 2 Channel A (debug interface) is operating properly. Tests include an Internal Loopback Test, Timer Tests, and UART Interrupt Tests. • Internal Loopback Test verifies 8-bit patterns can be written to the UART for transmitting. • Timer Tests verify that the timers increment correctly and generate interrupts as programmed. • UART Interrupt Tests verify the ability of the DUARTs to generate transmit ready and receive interrupts. This test includes: • Individual Channel Interrupts verify that an interrupt is sent from each channel when the UART is placed in transmit mode and when a character is sent. The test checks to make sure that no other spurious interrupts are generated. • Port Interrupts verify that each channel port can generate interrupts in loopback mode in parallel without affecting other channels. • Interrupt Test with One Interrupt Enabled verifies the UART send and receive interrupts. • Interrupt Test with One Interrupt Disabled verifies that the UART is able to clear interrupts. • Interrupts Disabled verifies that interrupts do not occur if they have been disabled. IPG-SPI Dual Port RAM Interrupt/Synchronized Tests - This test verifies the proper operation of the SPI interface DPR. Interrupts generated from the IPG are IPG-SPI interrupts. Interrupts generated from the SPI are SPI-IPG interrupts. These tests include an IPG-SPI Interrupt Test, an SPI-IPG Interrupt Test and a Synchronous Access Test: IPG-SPI Interrupt Test is composed of three checks: External Interrupt Check, Interrupt Disable Check, and Interrupt Generation Check. At the beginning of these tests, the SPI Global Interrupt Enable (GIE) control bit, the Status Register and Interrupt Enable (IE) and Interrupt Flag (IF) Registers are all cleared. This test checks the ability of the SPI to receive interrupts from the IPG. • External Interrupt Check verifies that no external device is continuously generating interrupts. If the content of the IF register is not zero after initialization, a failure occurs. • Interrupt Disable Check verifies that the GIE bit and IE register can disable all interrupts. • Interrupt Generation Check verifies that an internal interrupt can be generated and received properly. It also verifies that the interrupt cycle clears the IF bit, but not the GIE bit. SPI-IPG Interrupt Test is also composed of the above three checks. However, the IPG GIE control bit, the Status Register and IE and IF registers are cleared. This test checks the ability of the IPG to receive interrupts from the SPI. Synchronous Access Test verifies that the IPG and SPI processors can access DPR simultaneously.
WARP Local	Test time is ~25 seconds. This set of tests verifies the functionality of the WARP processor. The WARP is downloaded with diagnostics code which is then executed under control of the IPG CPU. The following is a list of the tests included in this set. Internal RAM Test and Processor RAM Test - Although these RAM exist in different locations, each of these tests use the same three subtests to verify RAM operation: a pattern test, an address test and a 1's/0's test. The pattern test uses 55555555, AAAAAAAA, 333333333, 0F0F0F0F, 00FF00FF, 0000FFFF patterns to verify that each bit in RAM can be set and reset. The address test uses 31-bit long

	word addresses which are written and checked to verify the address lines are performing correctly. Finally, the sliding 1's/0's test verifies that proper setting and clearing of bits occurs and erroneous writes to blocks of memory does not occur. Refer to Section 1-4-2, Memory Menu, Table 1-4 for more information about the sliding 1's/0's test (a.k.a. Sliding 1's/0's). Timer Test - This test verifies that the internal timers in the WARP CPU are operational. This test checks for the ability of the timers to count linearly and to provide interrupts to the CPU. Interrupt Test - This test verifies the proper operation of the WARP CPU Interrupts. It is comprised of three checks: External Interrupt Check, Interrupt Disable Check, and Interrupt Generation Check. At the beginning of these tests, the Global Interrupt Enable (GIE) control bit, the status register and Interrupt Enable (IE) and Interrupt Flag (IF) registers are all cleared. • External Interrupt Check verifies that no external device is continuously generating interrupts. If the content of the IF register is not zero after initialization, a failure occurs. • Interrupt Disable Check verifies that the GIE bit and IE Register disables all interrupts. • Interrupt Generation Check verifies that an internal interrupt can be generated and received properly. It also verifies that the interrupt cycle clears the IF bit, but not the GIE bit. DMA Test - This test verifies that the on-chip DMA controller is functioning properly. The DMA transfer occurs from one section of Processor RAM to another section of Processor RAM. This test contains three subtests: DMA Data Transfer Test, DMA Interrupt Test, and DMA Synchronization Test. • DMA Data Transfer Test verifies that all data can be transferred accurately. • DMA Interrupt Test verifies that a DMA Interrupt can be generated and received properly. • DMA Synchronization Test verifies that a data transfer can be synchronized with interrupts.
SPU DPR Sync	Test time is ~12 seconds. This test verifies that the IPG CPU and SPU can access the DPR at the same time. The test instructs the SPU to write a hex pattern (AAAAAAAA) into the upper half of the DPR. An interface function writes a different hex pattern (55555555) into the lower half of the DPR. The interface function checks for the correct data in both halves of the DPR.
SPI DPR Sync	Test time is ~11 seconds. This test verifies that the IPG CPU and SPI can access the DPR at the same time. The test will instruct the SPI to write a hex pattern (AAAAAAAA) into the upper half of the DPR. An interface function writes a different hex pattern (55555555) into the lower half of the DPR. The interface function will check for the correct data in both halves of the DPR.
SPU-SPI DPR Sync	Test time is ~20 seconds. This test verifies that the SPU and SPI can access the DPR at the same time. The test instructs the SPU to write a hex pattern (AAAAAAAA) into the upper half of the DPR. The SPI will be instructed to write a different hex pattern (55555555) into the lower half of the DPR. The SPI checks for the correct data in both halves of the DPR.
SPU Interrupt	Test time is ~7 seconds. This test verifies the functionality of IPG CPU-SPU DPR interrupts. This DPR can be accessed from both the IPG CPU and the SPU CPU. Interrupts generated from the IPG are IPG-SPU interrupts. Interrupts generated from the SPU are SPU-IPG interrupts. These tests include an IPG-SPU Interrupt Test and a SPU-IPG Interrupt Test. IPG-SPU Interrupt Test verifies the reception of the IPG CPU DPR interrupts by the SPU processor. This test disables SPU interrupts and writes to an SPU interrupt location. If the Interrupt Flag (IF) Register shows any interrupts occurring, an error is logged. This test then enables the IPG CPU interrupt and writes to the SPU DPR interrupt location to cause an expected interrupt. If there are no interrupts recorded by the SPU, an error is logged. SPU-IPG Interrupt Test verifies the reception of the SPU DPR interrupts by the IPG processor. This test is composed of three checks: External Interrupt Check, Interrupt Disable Check, and the Interrupt Generation Check. At the beginning of these tests, the SPU 's Global Interrupt Enable (GIE) control bit, the Status Register and Interrupt Enable (IE) and Interrupt Flag (IF) Registers are all cleared. This test checks the ability of the SPU to receive interrupts from the IPG. • External Interrupt Check verifies that no external device is continuously generating interrupts. If the content of the register is not zero after initialization, a failure occurs. • Interrupt Disable Check verifies the GIE bit and IE Register can disable all interrupts. • Interrupt Generation Check verifies that an internal interrupt can be generated and received properly. It also verifies that the interrupt cycle clears the IF bit, but not the GIE bit.
SPI Interrupt	Test time is ~18 seconds. This test verifies the functionality of IPG CPU-SPI DPR interrupts. This DPR can be accessed from both the IPG CPU and the SPI CPU. Interrupts generated from the IPG are IPG-SPI interrupts. Interrupts generated from the SPI are SPI-IPG interrupts.

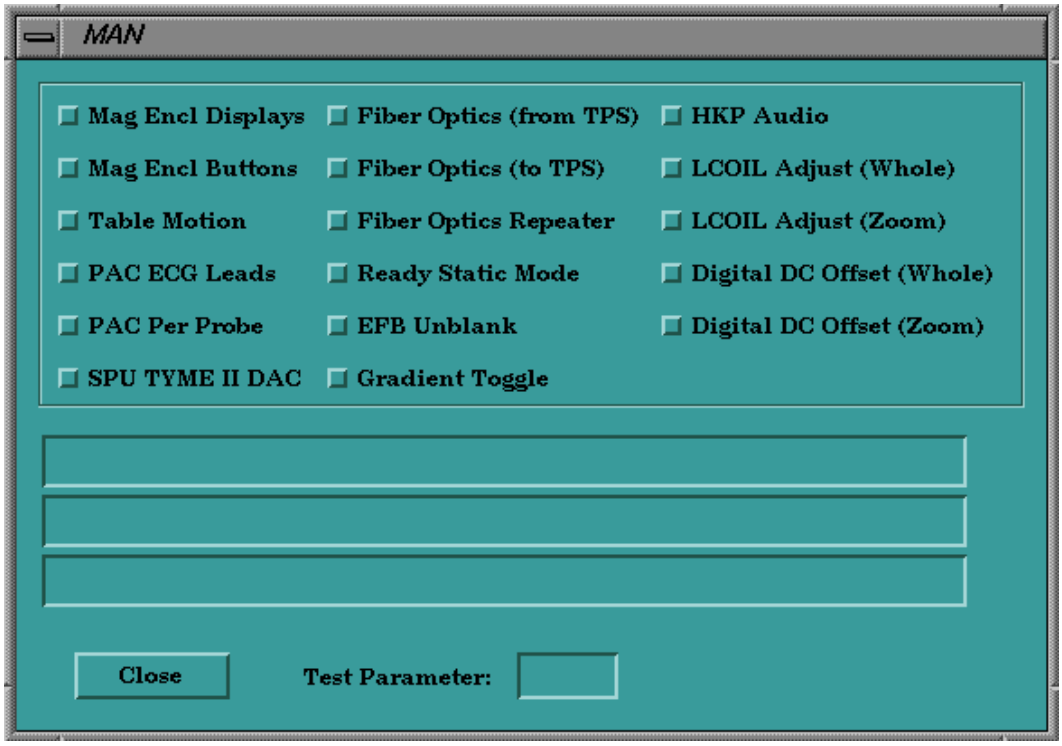
	IPG-SPI Interrupt Test verifies the reception of the IPG CPU DPR interrupts by the SPI processor. This test disables SPI interrupts and writes to an SPI interrupt location. If the Interrupt Flag (IF) Register shows any interrupts occurring, an error is logged. This test then enables the IPG CPU interrupt and writes to the SPI DPR interrupt location to cause an expected interrupt. If there are no interrupts recorded by the IPG, an error is logged. SPI-IPG Interrupt Test verifies the reception of the SPI DPR interrupts and SPI Watchdog interrupts by the IPG processor. This test is composed of: External Interrupt Check, Interrupt Disable Check, and Interrupt Generation Check. These tests check both the SPI DPR and Watchdog interrupts. At the beginning of these tests, the SPI Global Interrupt Enable (GIE) control bit, the Status Register, Interrupt Enable (IE) and Interrupt Flag (IF) Registers are cleared. • External Interrupt Check verifies that no external device is continuously generating interrupts. If the content of the IF register is not zero after initialization, a failure occurs. • Interrupt Disable Check verifies that the GIE bit and IE Register disables all interrupts. If they do not, a failure occurs. • Interrupt Generation Check verifies that an internal interrupt can be generated and received properly. It also verifies that the interrupt cycle clears the IF bit, but not the GIE bit.
WARP Interrupt	Test time is ~5 seconds. This test verifies the functionality of IPG CPU-WARP interrupts. The DPR can be accessed from both the IPG CPU and the WARP CPU. Interrupts generated from the IPG are IPG-WARP interrupts. Interrupts generated from the WARP are WARP-IPG interrupts. IPG-WARP Interrupt Test verifies the reception of the IPG CPU DPR interrupts by the WARP processor. This test disables WARP interrupts and writes to a WARP interrupt location. If the Interrupt Flag (IF) Register shows any interrupts occurring, an error is logged. This test then enables the IPG CPU interrupt and writes to the WARP DPR interrupt location to cause an expected interrupt. If there are no interrupts recorded by the IPG, an error is logged. WARP-IPG Interrupt Test verifies reception of the WARP DPR interrupts and WARP Watchdog interrupts by the IPG processor. This test is composed of: External Interrupt Check, Interrupt Disable Check, and Interrupt Generation Check. These tests check both the WARP DPR and Watchdog interrupts. At the beginning of these tests, the WARP Global Interrupt Enable (GIE) control bit, the Status Register, Interrupt Enable (IE) and Interrupt Flag (IF) Registers are cleared. • External Interrupt Check verifies that no external device is continuously generating interrupts. If the content of the IF register is not zero after initialization, a failure occurs. • Interrupt Disable Check verifies that the GIE bit and IE Register disables all interrupts. If they do not, a failure occurs. •Interrupt Generation Check verifies that an internal interrupt can be generated and received properly. It also verifies that the interrupt cycle clears the IF bit, but not the GIE bit.
SPU-SPI Interrupt	Test time is ~12 seconds. This test verifies the functionality of SPU-SPI DPR interrupts. This DPR can be accessed from both the SPI and the SPU. Interrupts generated from the SPI are SPI-SPU interrupts. Interrupts generated from the SPU are SPU-SPI interrupts. These tests include an SPU-SPI Interrupt Test and an SPI-SPU Interrupt Test. SPU-SPI Interrupt Test verifies the reception of the SPU processor DPR interrupts by the SPI processor. This test disables SPI interrupts and writes to an SPU interrupt location. If the Interrupt Flag (IF) Register shows any interrupts occurring, an error is logged. This test then enables the SPU processor interrupt and writes to the SPI DPR interrupt location to cause an expected interrupt. If there are no interrupts recorded by the SPU, an error is logged. SPI-SPU Interrupt Test verifies the reception of the SPI processor DPR interrupts by the SPU processor. This test is identical to the SPU-SPI Interrupt Test with the SPI and SPU reversed.
SPI-TYME Loopback	Test time is ~15 seconds. This test verifies the proper operation of the SPI to TYME board to GCP data paths. TYME Loopback Test - This test verifies the proper operation of the SPI to TYME Board and TYME Board to GCP data paths. The TYME Board is used to interface between the SRI and SPI and interface between the GCP and SPI. The IPG sets up the TYME Board ready for

	loopback. The SPI generates 8-bit patterns (55, AA, 33, 00, FF) which will get bounced back to the TYME Board. The SPI verifies the patterns and reports any errors to the IPG CPU. The same process is repeated for the GCP, connected via the second channel of UART1. Console Loopback Test - This test verifies the proper operation of the SPI to TYME Board to GCP data paths. The IPG sets up the TYME Board to allow test patterns to be written to the GCP. The SPI then generates packets including 8-bit patterns (ox55, 0xAA, 0x33, 0x0F) that are sent to the GCP. The GCP then inverts the data and returns it to the SPI. If any errors occur, they are reported to the IPG CPU.
SPI-GPC Loopback	Test time is ~9 seconds. This test verifies the communication between the SPI and GCP and the corresponding serial path. The SPI transfer a communication packet to the GCP containing an Invert-and-Loopback opcode and 8-bit patterns (55, AA, 33, 00, FF). The information returned by the GCP is verified by the IPG.
PAC-TYME Loopback	Test time is ~20 seconds. This test verifies the communication path from the SPU to the TYME interface card. The SPU transfers a communication packet to the PAC (via the TYME Board) containing 8-bit test patterns (55, AA, 33, 00, FF). The information returned by the TYME Board is verified by the IPG.
PAC Loopback	Test time is ~21 seconds. This test verifies the communication between the SPU and PAC and the corresponding serial path. The SPU transfers a communication packet to the PAC (via the TYME Board) containing an Invert-and-Loopback opcode and 8-bit test patterns (55, AA, 33, 00, FF). The information returned by the PAC is verified by the IPG.
PAC Power-up	Test time is ~21 seconds. This test verifies the communication between the SPU and PAC and the corresponding serial path. The SPU transfers a communication packet to the PAC (via the TYME Board) containing an Invert-and-Loopback opcode and 8-bit test patterns (55, AA, 33, 00, FF). The information returned by the PAC is verified by the IPG.
PAC Gain	This test verifies that the Respiration Voltage Gain is functioning properly. The test reads the current Respiration Circuit voltage. The AGC circuit is doubled and the Respiration Circuit voltage read once more. If the new Respiration Circuit voltage is not also doubled, an error message is sent to the message log.
SPI-WIM Loopback	This test checks the connection from the SPI to the WIM by sending a test packet which the WIM, if present and functional, inverts and sends back to the SPI. The SPI verifies the data.
SPI-HKP Loopback	The HKP Datapath test, called from the monitor screen, simply sends a watchdog packet to the HKP. If the ack message is not returned within a time-out period, an error is logged and printed out to the monitor screen. Otherwise, a ``test successful" message is printed out to the monitor screen.
SPI-IWS Loopback	This test verifies the connection from the SPI to the WIM to the IWS PC by sending and receiving loopback data. Note that the SPI-WIM Loopback test tests the intermediate path from the SPI to the WIM, while this test checks the connection to the IWS-PC.
SPI-JPB Reset	This test updates the current waveform reset state, and also updates the current waveform freeze state so that no window is frozen and reset at the same time. It then uses the forward_cpb() routine to forward the waveform reset packet to the CPB. The forward_cpb() routine only forwards the packet to the CPB if the CPB is not busy.
SPI-HKP Reset	This test updates the current waveform reset state, and also updates the current waveform freeze state so that no window is frozen and reset at the same time. It then uses the forward_cpb() routine to forward the waveform reset packet to the CPB. The forward_cpb() routine only forwards the packet to the CPB if the CPB is not busy.
LCA Sequencer	This test executes the sequencer can correctly generate stepped waveforms, and that the sequencer waveform and instruction memory can be accessed while the sequencers play out waveform data. The WARP must be loaded with its diagnostics driver file for this test. The 020 downloads a configuration file, using the peripheral loader, and then loads a test program into sequencer memory to generate one sequence of stepped waveforms. The sequence consists of a number of instructions to exercise the LCA counters, and to allow the 020 time to perform a simultaneous access test of sequencer RAM. The WARP is set up to collect the waveform data generated; the data are not sent out for this test. The 020 sets the Instruction Start Address registers for each LCA and write the SSI Enable command to the master sequencer, initiating the test. While the waveforms are being generated, the 020 verifies that it can simultaneously access sequencer memory by performing write/read pattern tests of individual sequencer memory locations (excluding the addresses that contain the test program instructions and waveforms). When the EOS Interrupt is received by the 020, it stops testing sequencer memory and retrieves and verifies the last set of waveform data collected by the WARP. The LCAs are reset to end the test.
LCA Hammer	The purpose of this test is to force the Sequencer Instruction and Waveform memory banks to perform at their maximum bandwidths. Even though all nine sequencers are running at maximum bandwidth, only the X, Y, and Z gradient sequencers are monitored by this test. The WARP

	monitors the waveform and scalar values from the gradient sequencers. To date, this has been sufficient to detect numerous LCA timing and noise problems with the sequencers.
SRI Power-up	The purpose of this test is to force the Sequencer Instruction and Waveform memory banks to perform at their maximum bandwidths. Even though all nine sequencers are running at maximum bandwidth, only the X, Y, and Z gradient sequencers are monitored by this test. The WARP monitors the waveform and scalar values from the gradient sequencers. To date, this has been sufficient to detect numerous LCA timing and noise problems with the sequencers.
SRI EX RAM	SRI RAM Test (Fatal) – On power up, the last 512 bytes of RAM, locations FE00H -FFFFH are tested without destroying the application contents of the RAM. The SRI interrupts are disabled for this test. These locations are tested one at a time. The contents of a location are read, inverted, and written back to the location. The location is read again and compared to the value written. The original contents of the location are then written back to the location that has been tested.
SRI Encoder	Encoder Voltage Test – This test verifies that the voltage across the encoder (measured at SRI) is >4.0V.
SRI Pulse Width MOD	This test verifies that the Pulse Width Modulator is converting pulses to analog voltages correctly.
Grad Link Hammer	The purpose of this test is to have the WARP output known gradient data at the maximum rate while the GAP continuously monitors the gradient data. The SPU also monitors the gradient data. The timing of the WARP and SPU code is adjusted to duplicate the timing of applications code as much as possible. This test tries to detect spurious gradient data errors in the IPG and/or TYME boards.
SRI Loopback	Test time is approximately 9 seconds. This test verifies the communication between the SPI and the SRI and the corresponding serial path. The SPI transfers a communication packet to the SRI (via the TYME Board) containing an Invert-and-Loopback opcode and 8-bit test patterns (55, AA, 33, 00, FF). The information returned by the SRI will be verified by the IPG.
Grad Data Register	Test time is approximately 9 seconds. This test verifies the communication between the SPI and the SRI and the corresponding serial path. The SPI transfers a communication packet to the SRI (via the TYME Board) containing an Invert-and-Loopback opcode and 8-bit test patterns (55, AA, 33, 00, FF). The information returned by the SRI will be verified by the IPG.

6-2 IPG MAN Menu Test Descriptions

See Illustration 6-2 for IPG MAN (Manual) Menu options. Refer to Table 6-2 for test descriptions.



IPG MAN MENU
ILLUSTRATION 6-2

Note: An ICONTROL MODE test is available only for systems with 8645 Gradient Amps.

For a ***TwinSpeed*** scanner, there are two LCOIL and Digital DC Offset tests.

TABLE 6-2
IPG MAN TEST DESCRIPTIONS

TEST NAME	TEST DESCRIPTION
Magnet Enclosure Display	This test turns on the annunciators and seven segment displays on the magnet enclosure for verification by the service technician. When the test is requested from the host, the IPG diags exec will call a SPI interface function to load a SPI driver file and pass it a command to run the Magnet Enclosure Display Test. The SPI then sends a command to the SRI to run the test, which it does by cycling through the following series of actions in a continuous loop: it turns on all enclosure annunciators and fills the Scan Time and Table Motion Displays on the enclosure with 88:88. After a short delay, it turns all the displays off, and then turns each display on and off in sequence around the enclosure. Then it turns them all on again, and repeats the cycle indefinitely for the technician to observe. The exact delays are determined as the test is implemented. When you wish to end the test, choose a Stop Test selection on the plasma panel. The host diagnostics process passes a stop command packet to the IPG diags exec, which passes the command on to the SPI via an interface function. The SPI instructs the SRI to blank all enclosure displays, ending the test.
Magnet Enclosure Buttons	This test verifies the operation of the control buttons on the magnet enclosure and the reception of these inputs by the IPG. Key entry by a service technician is required for this test. This test is run in an identical manner to the Magnet Enclosure Display test, except that the SRI performs button testing in its continuous loop. In this loop, the SRI awaits keystroke entries from the magnet enclosure buttons. All buttons are assigned a unique number. When a keystroke is received, the SRI displays the number of the keystroke received and the number of times it has received this button selection in the Scan Time and Table Motion Display Windows on the enclosure.
Table Motion	This test moves the moves the cradle into the magnet bore, and then returns it to its starting position. When this test is run, the cradle is automatically moved into the magnet bore a maximum distance of 500 mm, then is returned to its starting position. Any error messages generated during this test are stored in the Error Message Log.
PAC ECG Leads	This test checks the functionality of all the ECG leads. All of the clip leads are connected together. The right leg (RL) lead supplies a +2.5V dc drive signal to the right arm (RA), left arm (LA), and left leg (LL) leads. The signal from each of these leads is read in turn, and checked that their respective inputs to the ECG A/D converter are in range +2.5V to +200mv. If any of these leads is not in this range, an error message is entered into the Message Log. If the signals from the RA, LA, and LL leads are all out of range, it is assumed that the RL lead has failed.
PAC Per Probe	Test time is ÷ 0.1 second. This test verifies that the LED in the peripheral probe is functioning properly. The test measures the voltage across the LED from the A/D converter. If the voltage is >A67H (+1.5V) or <8CCH (+0.5V), it is assumed that the diode is either failing or disconnected. Any errors are sent to the message log.
SPU TYME DAC	This test sends some basic waveforms, generated locally from the SPU, out from its serial port through the TYME card D/A converter. The service technician can connect a scope probe to the output of the DAC to monitor the output. The waveforms consist of linear ramping patterns of differing frequencies. Unexpected rugged steps and spikes are the indications of failure.
Fiber Optics (from TPS)	Selecting this test causes the fiber optic cables outgoing from the TPS to be lit. This includes the PAC transmit, SRI transmit, SRI Reset, and MDS output lines. They can then be inspected, and the light intensity measured using the light instrument. The button must be pressed again to end the test. Selecting this test also causes the fiber optic cables returning to the TPS to be lit. This includes the SRI receive and PAC receive lines. The test button must be pressed BEFORE disconnecting the cable to perform the inspection. (This is because the software must send the signal to the PAC and SRI to drive their return lines, before breaking that connection for inspection.) The return lines can then be inspected, and the light intensity measured using the light instrument. The button must be pressed again to end the test. (The lines must be reconnected following inspection, before pressing the button to end the test.)
Fiber Optics (to TPS)	Selecting this test causes the fiber optic cables outgoing from the TPS to be lit. This includes the PAC transmit, SRI transmit, SRI Reset, and MDS output lines. They can then be inspected, and the light intensity measured using the light instrument. The button must be pressed again to end the test.

	Selecting this test also causes the fiber-optic cables returning to the TPS to be lit. This includes the SRI receive and PAC receive lines. The test button must be pressed BEFORE disconnecting the cable to perform the inspection. (This is because the software must send the signal to the PAC and SRI to drive their return lines, before breaking that connection for inspection.) The return lines can then be inspected, and the light intensity measured using the light instrument. The button must be pressed again to end the test. (The lines must be reconnected following inspection, before pressing the button to end the test.)
Fiber Optics Repeater	The fiber optic repeater test is provided to test the loopback jumper and, thus, check the lines between the system cabinet and the repeater board. Before you run this test, set the loopback jumper to its loopback position. When the test runs, the IPG sends a data pattern out to the repeater board, and verifies that the exact same data is looped back to the IPG. Any mismatches indicate that either the loopback jumper is not set, or there is a fault in the lines between the IPG and the repeater boards.
VCONTROL Mode	For the VCONTROL MODE test description, see section 8 in the Gradient Driver Functional Tests.
GRAM Mode	For the GRAM MODE test description see section 8 in the Gradient Driver Functional Tests.
EFB Unblank	This manual test is verified by using an oscilloscope; it checks the output of the Envelope Feedback and RF Unblank signals coming from the TYME II board. UNBLANK1, UNBLANK2, EFB1 and EFB2 are played out at different duty cycles, so you can verify that these signals are being generated from the IPG and transmitted by the TYME II board.
Gradient Toggle	This manual test is verified using an oscilloscope. A series of patterns are played out over the x, y, and z gradients. The patterns are staggered such that the user can verify different sequences coming from each gradient. This verifies that the TYME II board is properly differentiating and transmitting each gradient's data,
HKP Audio	Hard Key Processor for the keyboard checks
Lcoil Adjust (Whole/Zoom)	An appropriate set of tolerances is chosen for each Gradient Coil. For ***TwinSpeed***, **WHOLE-BODY** and **ZOOM** GradModes are to be tested separately Refer to the Gram Tuning procedure for the proper cabinet type under Setup and Cals
Digital DC Offset (Whole/Zoom)	An appropriate set of tolerances is chosen for each Gradient Coil. For ***TwinSpeed***, **WHOLE-BODY** and **ZOOM** GradModes are to be tested separately Refer to the Gram Tuning procedure for the proper cabinet type under Setup and Cals

6-3 IPG MDS Menu Test Descriptions

See Illustration 6-3 for IPG MDS (Multi Drop Serial Link) Menu options. Refer to Table 6-3 for test descriptions.

IPG MDS TEST MENU
ILLUSTRATION 6-3

For a ***TwinSpeed*** scanner, there are two Gradient Driver Tests.

TABLE 6-3

IPG MDS TEST DESCRIPTIONS

TEST NAME	TEST DESCRIPTION
MDS Link	Test time is ~10 seconds. This test verifies that the MDS fiber optic circuit is complete, and it checks the initial status of the peripherals presently on the link. The test first checks the serial port on the SPI processor by transmitting test patterns (AAH, 55H, 33H, 0fH) and verifying them as they return from the loopback. Next, the SPI sends out four data bytes in succession to ensure that the MDS link is complete. An error message is logged if either test fails.
MDS Device Poll	Test time is ~7 seconds. This test verifies the operation of the GAP Board on the MDS Fiber Optic Link. The SPI addresses only two MDS Fiber Optic Link boards at a time. If the GAP does not transmit an error packet back to the SPI within two seconds, the test fails, and an error is logged.
RF Amp	Test time is ~6 seconds. This test verifies the operation of the MDS Link and the presence of the ERBTEC RF Amplifier. To verify its presence, the Command Register is addressed and read by the SPI via the MDS. No additional tests are used.
Spectro RF Amp	Note: This test is present only on systems with the spectroscopy option. Test time is ~6 seconds. This test verifies the operation of the MDS Fiber Optic Link and the presence and operation of the Spectro RF Amplifier Interface Board. To verify its presence, the Command Register is addressed and read by the SPI on the IPG Board via the MDS. The test below is used to verify the functionality of the Spectro RF Amplifier. Spectro RF Amplifier Interface Board Register Test The register is read for a specific pattern. The pattern indicates that the RF amplifier is connected through P2201 to the Dynamic Disable Module.
TR DYN Register	Test time is ~9 seconds. This test verifies that the TR/Dynamic Disable Board is attached to the MDS Fiber Optic Link and is in working order. This test is comprised of the following subtests: Presence Test The SPI on the IPG Board addresses the command register on the TR/Dynamic Disable Board. If the board is not present, an error is logged. Coil Configuration Register Test The coil configuration register is tested by writing/readback of patterns AAH, 55H, 33H, and 0FH. Fault Reporting Disable Register Test The Fault Reporting Disable Register is tested by writing/readback of patterns AAH, 55H, 33H, and 0FH. TR Command Register Test The TR Command Register is tested by writing/readback of bits 00 (Enable), 01 (Service), 02 (Reset), and 07 (Reset Status Registers). After each bit is read, the bit is checked to see if it has been reset. Register Reset Tests The Dynamic Disable and TR Driver Board has two status registers: the TR/ID Status Register and the Dynamic Disable Status Register. These status registers are reset to 00H by setting bit 07 of the TR Command Register. After bit 07 of the TR Command Register is set, the Status Registers are checked to see if they are reset. Also, the Coil Configuration and Fault Reporting Disable Registers are each written with pattern FFH. Then, bit 02 of the TR Command Register is set, and these registers are checked to see if they have gone to 00H.
TR DYN Power	Test time is ~5 seconds. These tests verify the operation of the three power supplies (+15V, –15V, and +1000V) associated with the Dynamic Disable and TR Driver Board. The status of these power supplies is indicated by the fault register bits 05 (+15V), 06 (–15V), and 07 (+1000V). These bits are each sampled five times (with approximately 65 milliseconds between each sample). A failure is displayed if one of the power supplies is indicated as having failed five times in a row.
Multicoil	Note: This test is present only on systems with the multicoil option. Test time is ~5 seconds. This test verifies the operation of the MDS Fiber Optic Link and the presence and operation of the Multicoil Board. To verify its presence, the Command Register of the Dynamic Disable/TR Driver Board is read. To verify the functionality of the registers, a set of Multicoil Board Register tests are run simultaneously with patterns AA, 55, 33, OF. Any errors are logged to indicate the failing register.

Power Monitor	Note: This test is present only on systems with the multicoil option. Test time is ~5 seconds. This test verifies the operation of the MDS Fiber Optic Link and the presence and operation of the Multicoil Board. To verify its presence, the Command Register of the Dynamic Disable/TR Driver Board is read. To verify the functionality of the registers, a set of Multicoil Board Register tests are run simultaneously with patterns AA, 55, 33, OF. Any errors are logged to indicate the failing register.
Gradient Driver(Whole/Suppl)	An appropriate set of tolerances is chosen for each Gradient Coil (Whole/Suppl) Test time is ~1 minute. Gradient Driver Tests are a new way of testing the Gradient Driver subsystem. This group of hybrid tests exercises and tests the entire Gradient Driver subsystem with the nonproprietary power-up tests and the proprietary static and dynamic tests. The Gradient Driver Tests use the GASM (GRAM Analog Service Module), if present, and the ASM (Analog Service Module) to look at digital and analog signals within the Gradient Driver subsystem. The Gradient Driver Tests were designed to isolate a problem to a FRU, or a group of FRUs. The tests are easy to invoke. Errors are reported to the error log with extended informatin in the Extended Error Log (EEL). For more information on the EEL, see the procedure for the Gradient Driver Extended Error Log. Power-up diagnostics provide a set of tests to test the basic funcitionality of GAP, ASM, MIF, GASM, and GRAM control board. Power-up diagnostics are run automatically on every GAP reset. Gradient driver power-up diagnostics are part of the GAP boot sequence: the entire boot sequence does not take more than fifteen seconds. The power-up diagnostics are run during, and at the end of, the boot sequence to verify the integrity of the MIF, ASM, GASM, GAP hardware, and GRAM Control Board. The Gradient Driver Power Tests include: Flash Memory Checksum Test, DUART Test, SRAM Test, MIF Register Read/Write Test, (G)ASM Register Read/Write Test, GRAM Control Board Read/Write Test, and (G)ASM Local Reference Voltage Check. For more information on the Gradient Driver Tests (Gradient Tests), see the procedure for Gradient Driver Tests.
Digital Tuning	Refer to the procedure Digital Tuning Exponential Monitoring for a test description.
Grad Framing Error/Clock Stop	This test checks the ability of the GAP to detect and report framing errors and clock stop errors in the gradient data connections between the TYME II card and the GAP board. There are four fiber optic connections that route gradient data to the GAP: one for each axis (i.e., *x*, *y*, and *z*), and one that provides the gradient clock. The GAP is capable of detecting the following error conditions with respect to the gradient data: FRAMING ERRORS Each gradient data clock burst should contain EXACTLY 21 clock cycles. If not, a framing error has occurred. If enabled, a PIC interrupt will be generated which the GAP can detect and report. CLOCK STOP ERRORS A burst of 21 gradient clock pulses should occur every 4 µsec. A clock stop error occurs if the time between successive clock bursts exceeds 800 µsec. If enabled, a PIC interrupt will be generated which the GAP can detect and report. Framing errors are generated by enabling a special diagnostics feature of the IPG Sequencer LCAs. This feature causes the sequencers to output 22-cycle gradient clock bursts instead of 21-cycle bursts (which is defined as a framing error). Clock stop errors are easily generated by (you guessed it) stopping the gradient clock. When done, the GAP is polled (via the SPI) to see if it received the "framing error" and "clock stop" PIC interrupts. If not, an error is logged.
GSW Communication Test	GIP sends a series of patterns to GSW and expects to receive identical patterns as response.
GSW Functional Test	GIP .tries different switch combinations and checks for success.

7- TPS/ISE SIZING/CONFIGURATION CHECKS

The TPS/ISE diagnostics executive performs a quick hardware configuration check (certain boards/memory) whenever data path, board level diagnostics are run or if any download (applications or diagnostics) occurs. This information is maintained in a file referred to as the *TPS/ISE Configuration File*.

If incorrect data were entered into the system configuration file, the problem can be corrected by editing the information; the diagnostics should then no longer report the error. If the problem is not due to incorrect information in the system configuration file, then there are hardware problems that are preventing the diagnostics from auto-sizing the memory, or accessing the boards over the VME Bus in the TPS/ISE subsystem. At the end of a configuration check, the TPS/ISE configuration file is updated to reflect the actual hardware configuration.

7-1 TPS/ISE Diagnostic Board Checks

In addition, for certain board level tests, the TPS/ISE chassis is first checked to verify if all boards necessary for the selected tests are present. If any needed boards are missing or not responding, an error is reported to the Message Log.

REVISION HISTORY

REV	DATE	AUTHOR	PRIMARY REASONS FOR CHANGE
0	Jul 12, 1996	B. Schmidt	Initial release
1	Apr 20, 1998	K. L-P	Changes for Lx 8.2 release
2	Oct 14, 1999	M. Keber	Corrections to TPS Hardware tested illustration and Table Motion test description, added IPG-II to Local Test Indicators section, removed obsolete IWS PC section, added proprietary feature statements.
3	Jan 7, 2000	M. Keber	Two Tone test moved from Receiver to Exciter test screen with 8.3.
4	May 26, 2000	M. Jones	Added info on pre 8.4 release Cardiac and Neuro workstations to Note 1, Illustration 1.
5	Jul 13, 2000	D. Lipschutz	Changes for TRM coil support.
6	Jul 26, 2001	J.Gerber	Updated for TwinSpeed scanner for 9.0 release.