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1- OVERVIEW

This procedure describes the setup and calibration of the Communications Pin Driver (CPD) Board in the System Support Module (SSM) for the following:

- 1.0T and 1.5T RF/PEN II cabinet
- 1.0T & 1.5T RF/PDU cabinet
- 1.5T SRF cabinet

Note

See *Dynamic Disable / TR Driver board adjustments* procedure for systems with both RF and Penetration cabinets (4X to 5.4 Hardware). See *Pin Switch Driver Board Set Up And Calibration* procedure for RF/PEN cabinets (5.5 Hardware).

2- TOOLS AND INSTRUMENTS REQUIRED

No special test equipment is required to perform the calibration in **Section 4 - SSM CAL SWITCH** or **Section 8 - POWER MONITOR TYPE CONFIGURATION**. Special equipment may be required for completing the checks or adjustments in the subsequent sections. Refer to Table 2-1 for the equipment required ***if it is necessary*** to complete the adjustments or checks in these sections.

TABLE 2-1
REQUIRED TOOLS AND EQUIPMENT

Item	Description	Part Number
1.	100 MHz Scope	46-183029P61
2.	Digital Multimeter (DMM)	46-194427P49
3.	Pot Tweaker	46-194427P361

3 - PREREQUISITES

WARNING!

FAILURE TO PROPERLY CONFIGURE JUMPER JP1 ON THE HIGH VOLTAGE BOARD COULD POSSIBLY RESULT IN SNR DEGRADATION AND DYNAMIC DISABLE OR DIRECT DRIVE FAILURES.

The SSM High Voltage (HV) Board jumper, JP1, must be set to either the 1000V position for 1.5T or 500V position for 1.0T systems. This high voltage bias is for the Body 1 and Body 2 Dynamic Disable Circuits in the RF body coil and the Direct Drive Circuitry (DD) in the body hybrid splitter. Jumper JP1 should come preset for all new installations and should not require changing. If the HV board ever fails, however, and is replaced, the position of this jumper on the new board should be checked before it is installed.

4- TEST SWITCH AND TEST LED DEFINITIONS

The following Table lists the SSM Test Switch positions and Test LED Definitions. This table is referenced when using the Front Panel Switches sections.

TABLE 4-1
TEST SWITCH AND TEST LED DEFINITIONS

Task	Switch Number	Position	Item Controlled	LED Bank 1	LED Bank 2
Normal Operation:	1	Down		MDS comm status	Head T/R fault
	2	--------	(When one	NB comm status	Body T/R fault
	3	--------	of these 10 is in use, the others	Monitor A comm status	Spectro T/R fault
	4	--------	are inactive)	Monitor B comm status	Body Coil 1 fault
	5	--------		PS fault	Dyn Disable fault
	6	--------		top cover open	Body Coil 2 fault
	7	--------		MC faults disabled	Multi-coil 1 fault
	8	--------		T/R faults disabled	Multi-coil 2 fault
	9	--------		DD faults disabled	Multi-coil 3 fault
	10	--------		DD open ckt adj failure	Multi-coil 4 fault
Static Control of Drivers:	1	UP		Head T/R open	Dyn Disable open
	2	DOWN		Head T/R short	Dyn Disable short
	3	DOWN		Body T/R open	Multi-coil 1 short
	4	DOWN		Body T/R short	Multi-coil 1 open
	5	UP	MC1 drv enable	Spectro T/R open	Multi-coil 2 short
	5	DOWN	MC1 drv disable		
	6	UP	MC2 drv enable	Spectro T/R short	Multi-coil 2 open
	6	DOWN	MC2 drv disable		
T/Rs Disabled:	7	UP	MC3 drv enable	Body Coil 1 open	Multi-coil 3 short
	7	DOWN	MC3 drv disable		
	8	UP	MC4 drv enable	Body Coil 1 short	Multi-coil 3 open
	8	DOWN	MC4 drv disable		
	9	UP	Source Mode	Body Coil 2 open	Multi-coil 4 short
	10	UP			
	9	DOWN	Sink Mode	Body Coil 2 short	Multi-coil 4 open
	10	DOWN			

4- TEST SWITCH AND TEST LED DEFINITIONS (continued)

TABLE 4-1 (CONTINUED)
TEST SWITCH AND TEST LED DEFINITIONS

Task	Switch Number	Position	Item Controlled	LED Bank 1	LED Bank 2
Pulse Control of Drivers:	1	UP		Head T/R open	Dyn Disable open
	2	DOWN		Head T/R short	Dyn Disable short
	3	UP		Body T/R open	Multi-coil 1 short
	4	DOWN		Body T/R short	Multi-coil 1 open
	5	UP	MC1 drv enable	Spectro T/R open	Multi-coil 2 short
	5	DOWN	MC1 drv disable		
	6	UP	MC2 drv enable	Spectro T/R short	Multi-coil 2 open
	6	DOWN	MC2 drv disable		
	7	UP	MC3 drv enable	Body Coil 1 open	Multi-coil 3 short
	7	DOWN	MC3 drv disable		
	8	UP	MC4 drv enable	Body Coil 1 short	Multi-coil 3 open
	8	DOWN	MC4 drv disable		
	9	UP	Source Mode	Body Coil 2 open	Multi-coil 4 short
	10	UP			
	9	DOWN	Sink Mode	Body Coil 2 short	Multi-coil 4 open
	10	DOWN			
PS Override Tests	1	UP		Dock enable	--------
	2	DOWN		PAC 8V	--------
	3	DOWN		PAC 9V	–5V Supply too high
	4	UP			–15V Supply too high
	5	UP	Dock disable	Bore vent	+15V Supply too high
	5	DOWN	Dock enable		
	6	UP	PAC 9V	Patient Alignment Light	HV Sense too high
	6	DOWN	PAC 8V		
	7	UP	Bore light enable	Bore light	–5V Supply too low
	7	DOWN	Bore light disable		
	8	UP	PAL enable	--------	–15V Supply too low
	8	DOWN	PAL disable		
	9	UP	Bore vent enable	MCD enable	+15V Supply too low
	9	DOWN	Bore vent disable		
	10	--------		--------	HV sense too low

4- TEST SWITCH AND TEST LED DEFINITIONS (continued)

TABLE 4-1 (CONTINUED)
TEST SWITCH AND TEST LED DEFINITIONS

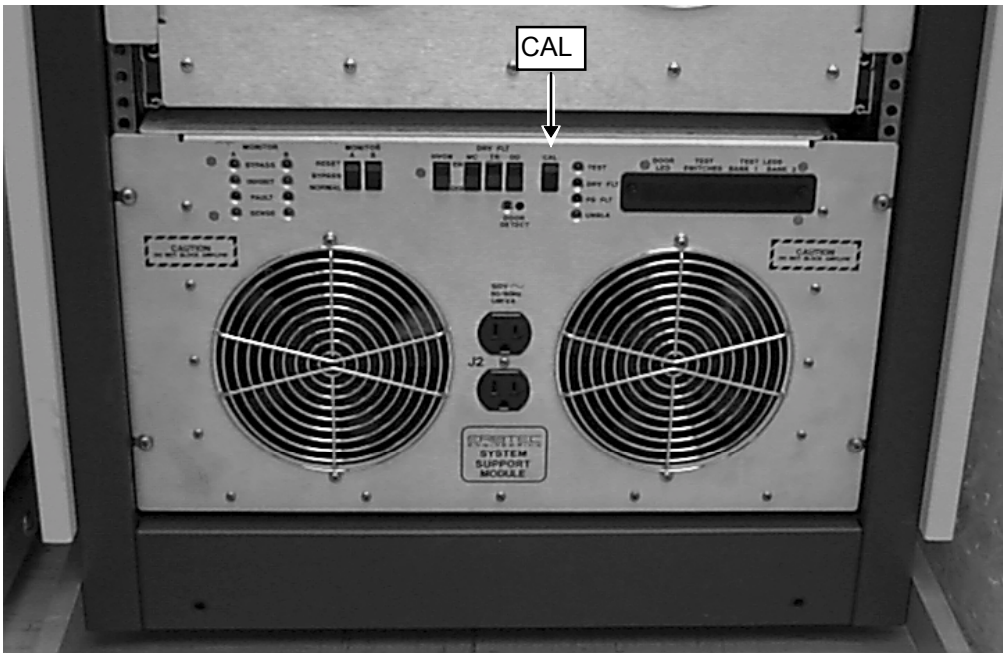
Task	Switch Number	Position	Item Controlled	LED Bank 1	LED Bank 2
				Monitor A	Monitor B
Monitor Fault Summary	1	UP		RF without unblank	RF without unblank
	2	UP		–15V Supply fault	–15V supply fault
	3	DOWN		Body Pwr limit fault	Body pwr limit fault
	4	UP		Head Pwr limit fault	Head pwr limit fault
	5	--------		Spectro Pwr limit fault	Spectro pwr limit fault
	6	--------		Duty Cycle fault	Duty cycle fault
	7	--------		RF Pulse Width fault	RF pulse width fault
	8	--------		+15V Supply fault	+15V supply fault
	9	--------		Body Cable fault	Body cable fault
	10	--------		Head/Spectro Cable fault	Head/spectro cable fault
Multi-coil Configuration	1	UP		Multi-coil 1 enable	--------
	2	DOWN		Multi-coil 2 enable	--------
	3	UP		Multi-coil 3 enable	--------
	4	UP		Multi-coil 4 enable	--------
	5	UP	MC1 enable	--------	--------
	5	DOWN	MC1 disable		
	6	UP	MC2 enable	--------	--------
	6	DOWN	MC2 disable		
	7	UP	MC3 enable	--------	--------
	7	DOWN	MC3 disable		
	8	UP	MC4 enable	--------	--------
	8	DOWN	MC4 disable		
	9	--------		--------	--------
	10	UP, then DOWN	Program	--------	--------
Monitor Type Configuration	1	UP		--------	--------
	2	UP		Monitor A 1.0T	Monitor B 1.0T
	3	UP		--------	--------
	4	UP		Monitor A 1.5T w/EFB	Monitor A 1.5T w/EFB
	5	UP, 6 DOWN=1.0T		--------	--------
	5	UP AND 6 UP=1.5T		--------	--------
	7	--------		--------	--------
	8	--------		--------	--------
	9	--------		--------	--------
	10	UP, then DOWN	Program	--------	--------

5- SSM CAL SWITCH

WARNING!

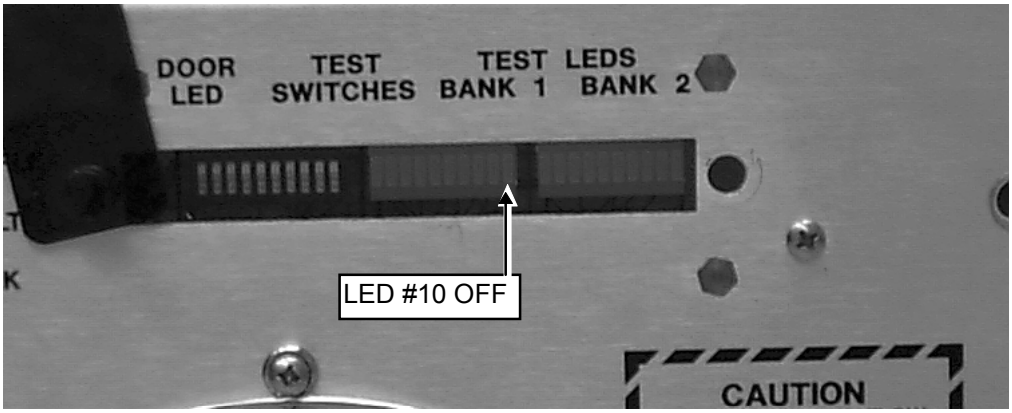
THE SSM WILL NOT FAULT IF IT IS CALIBRATED WITH A DISCONNECTION OR POOR CONNECTION TO ONE OF THE 4 MAGNET ROOM DYNAMIC DISABLE BIAS LINES (J72, J73, J75, AND J76 ON THE MAGNET ROOM SIDE OF THE PENETRATION PANEL). IMAGE SNR DEGRADATION WILL BE NOTICED BUT THE SSM MAY NOT FAULT. INSPECT THE FOUR BIAS LINE CONNECTIONS FROM THE PEN PANEL TO THE RF COIL BEFORE PERFORMING THIS CALIBRATION.

1. Press and release the CAL switch on the front of the SSM (see Illustration 5-1). This samples the open circuit fault detect signals and adjusts the threshold accordingly for the Dynamic Disable Circuits: J42 (Body 1), J43 (Body 2), and J44 (Direct Drive). When the CAL switch is pressed the LEDs labeled TEST, DRV FLT, and PS FLT will illuminate (this does not indicate a fault).



SSM CAL SWITCH LOCATION
ILLUSTRATION 5-1

2. View the front panel LEDs. Ensure the Bank 1, LED #10 is OFF (see Illustration 5-2). This LED indicates the adjustment process was successful.



SSM FRONT PANEL LEDs
ILLUSTRATION 5-2

6- TR VOLTAGE ADJUSTMENT WITH PULSE TRAIN

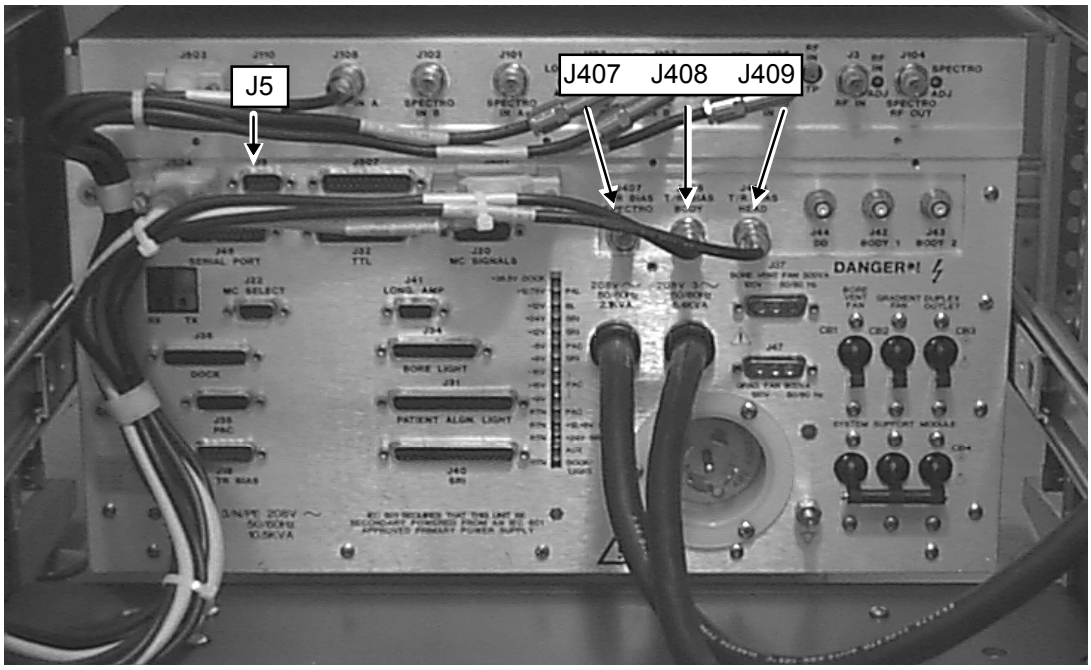
Note

The TR Voltages are factory set and should not require adjustment. This section was included for troubleshooting purposes and is not intended to be performed as a normal part of the calibration process.

6-1 Hardware Preparation

1. Extend the SSM chassis. Allow sufficient cable slack to avoid pinching or straining. Open the lids.

2. Verify cables (and their respective loads) are properly connected to J409 (Head TR) and J408 (Body TR); see Illustration 6-1.



CABLES LOCATIONS ON SSM
ILLUSTRATION 6-1

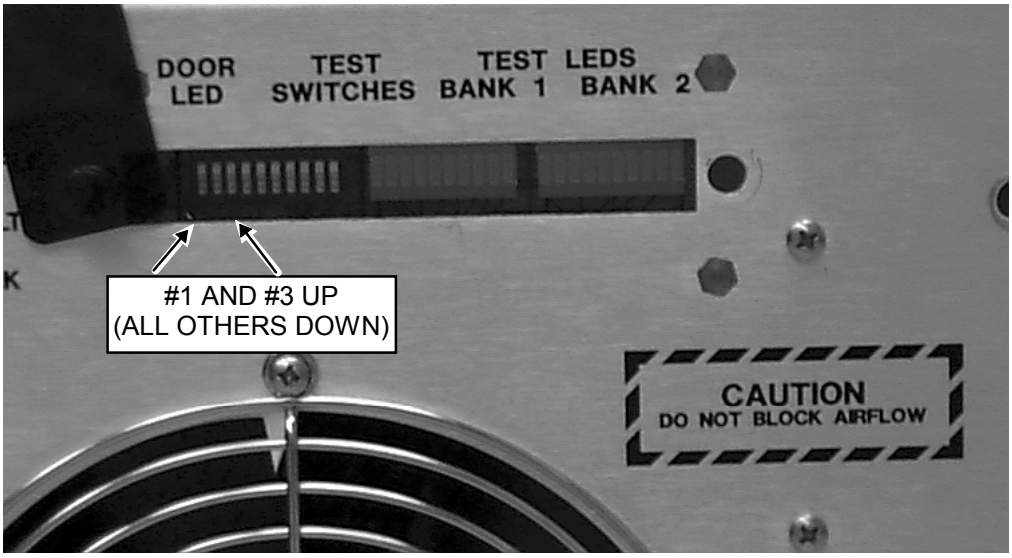
3. At the SSM disconnect J5 (UNBLK EN); see Illustration 6-1.

4. Configure the front panel DIP switches as shown in Illustration 6-2. This should generate a periodic unblank pulse train. Refer to Table 3-1 for the test switch and test LED definitions.

Note

Order of DIP switch placement is important, otherwise, system will not recognize changes. Place DIP Switch #3 in the UP position first and **then Switch #1** in the UP position. Entering test mode may cause RF Amp fault; this is normal and may be disregarded.

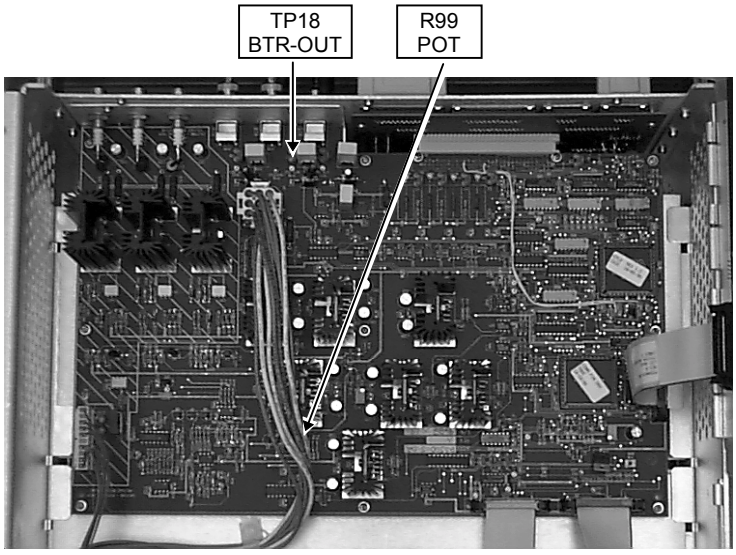
6-1 Hardware Preparation (continued)



DIP SWITCH CONFIGURATION
ILLUSTRATION 6-2

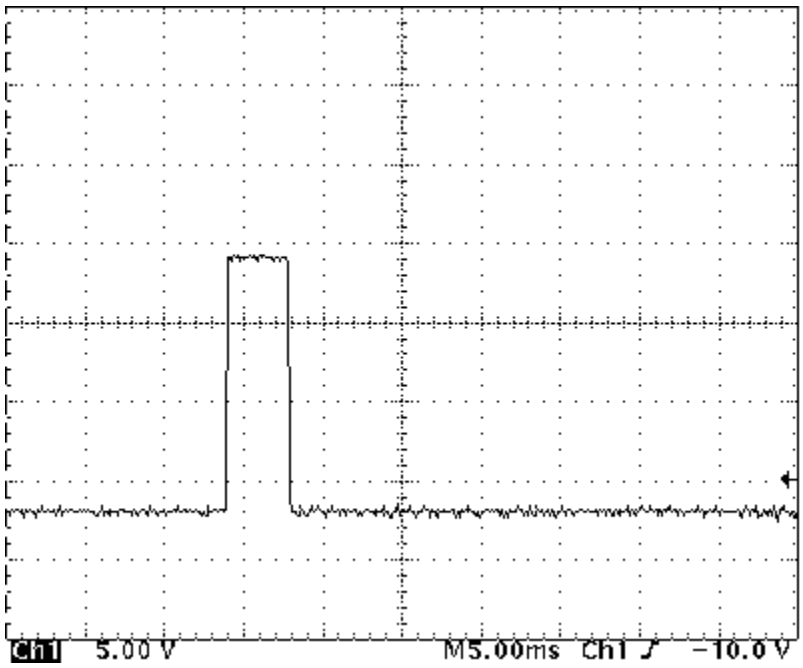
6-2 TR Voltage (Positive) Adjustments

1. Connect an oscilloscope to monitor the Body TR at TP18 (BTR-OUT); see Illustration 6-3. Adjust R99 until the positive going portion of the Body TR pulse is 4.00 VDC as referenced to ground level. See Illustration 6-4. The negative portion (not adjustable) will measure approximately -12.25 VDC as referenced to ground.



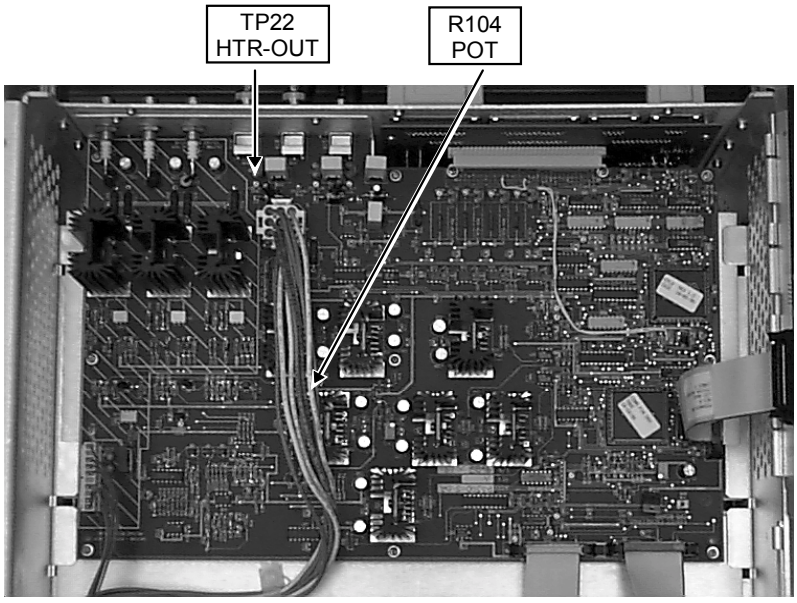
TR VOLTAGE ADJUSTMENT/BODY TR TEST POINT
ILLUSTRATION 6-3

6-2 TR Voltage (Positive) Adjustments (continued)



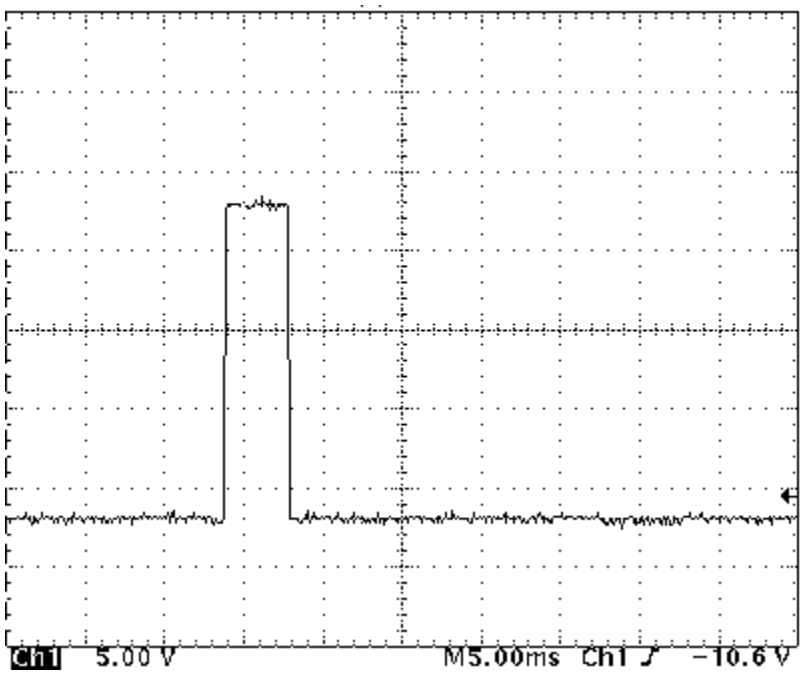
BODY TR SCOPE WAVEFORM SEEN AT TP18 (BTR-OUT)
ILLUSTRATION 6-4

2. Connect an oscilloscope to monitor the Head TR at TP22 (HTR-OUT); see Illustration 6-5. Adjust R104 until the positive going portion of the Head TR pulse is 8.00 VDC as referenced to ground level. See Illustration 6-6. The negative portion (not adjustable) will measure approximately -12.25 VDC as referenced to ground.



TR VOLTAGE ADJUSTMENT/HEAD TR TEST POINT
ILLUSTRATION 6-5

6-2 TR Voltage (Positive) Adjustments (continued)



HEAD TR SCOPE WAVEFORM SEEN AT TP22 (HTR-OUT)
ILLUSTRATION 6-6

Note

For Spectro TR adjustments please refer to the appropriate Spectroscopy (MNS) Subsystem Setup and Calibration Tab.

6-3 Cable and Test Switch Restoration

1. Place DIP switch #3 and #1 (respectively) in the Down position. Place all other switches in the Down position.

2. Reconnect J5 (UNBLK EN) at the rear of the SSM.

3. If not proceeding to next section, refer to **Section 10 - System Restoration**.

7- MULTI-COIL OPTION

Note

Disabling is not normally required (even on systems without the Multi-Coil Option). Each SSM (CPD Board) is shipped from the factory with all four Multi-Coil Drivers enabled. This section was included mainly for troubleshooting purposes and should not need to be performed as a part of the normal calibration process.

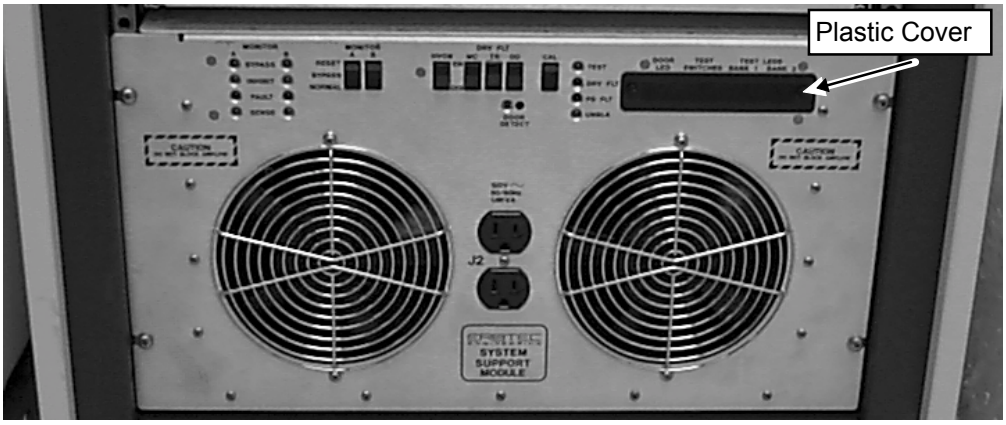
7-1 Multi-Coil Driver Enable/Disable

The Multi-Coil Drivers can be enabled and disabled in one of two ways: an alternate proprietary GE procedure or via the front panel switches (Section 7-1-1).

The setting should be verified if the spare board seal is broken.

7-1-1 Via the Front Panel Switches

1. Remove the plastic cover from the Test Switch and Test LEDs window on the front of the SSM. See Illustration 7-1.



TEST SWITCH AND TEST LEDs WINDOW
ILLUSTRATION 7-1

Note

Place DIP Switch #1 in the UP position last. Order of DIP switch placement is important otherwise system will not recognize changes.

2. Place switches 3, 4, and 1 in the Up position. Ensure that all other switches are in the Down position.

3. To program the correct Multi-Coil Driver configuration to the CPD Board, perform one of the following steps. This procedure references Table 4-1, Multi-Coil Driver Configuration.
   a. To disable all Multi-Coil Drivers, place switches 5, 6, 7, & 8 in the Down position and proceed to step 4.
   b. To disable Multi-Coil Drivers 3 & 4, place switches 5 & 6 in the Up position and proceed to step 4.
   c. To enable all Multi-Coil Drivers, place switches 5, 6, 7, & 8 in the Up position and proceed to step 4.

7-1-1 Via the Front Panel Switches (continued)

4. Place switch #10 in the Up position.

5. Place switch # 10 in the Down position. Bank 1 LEDs 1, 2, 3, & 4 are illuminated and remain illuminated once switch #10 is in Down position.

6. Place switch #1 in the Down position. Bank 1 LED 1 will illuminate for approximately one minute, then extinguish.

7. Place all switches in the Down position.

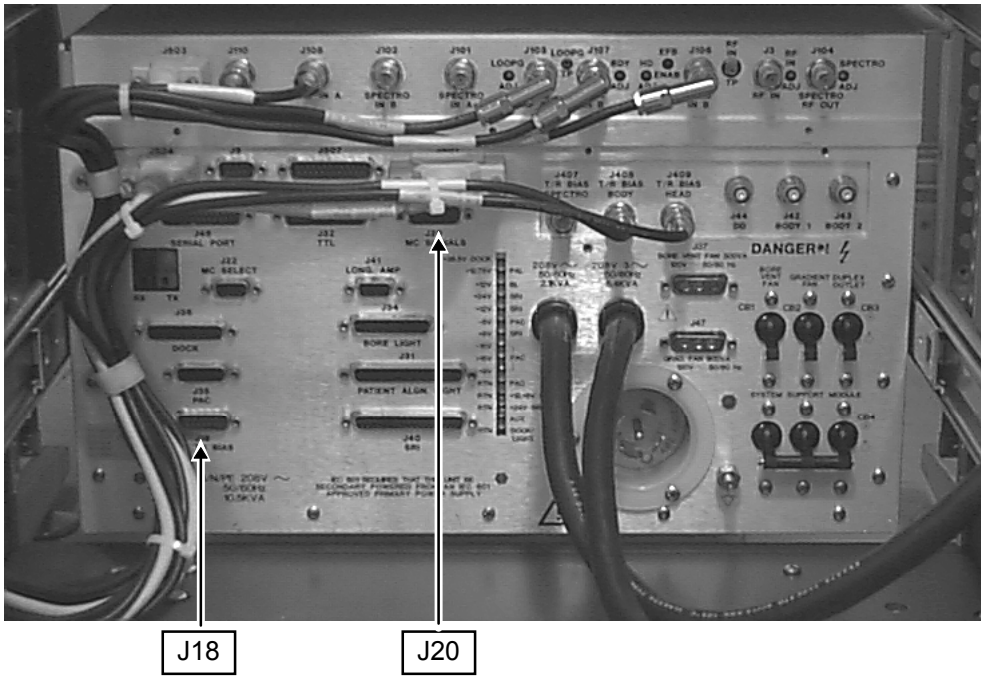
8. Cycle the main circuit breaker power at the SSM by turning CB4 to the OFF position, waiting 15 seconds, then setting CB4 to the ON position. This step saves the changes to the SSM.

9. Replace the plastic cover on the front of the SSM.

7-2 Multi-Coil –5 VDC Power Supply Adjustments

Note

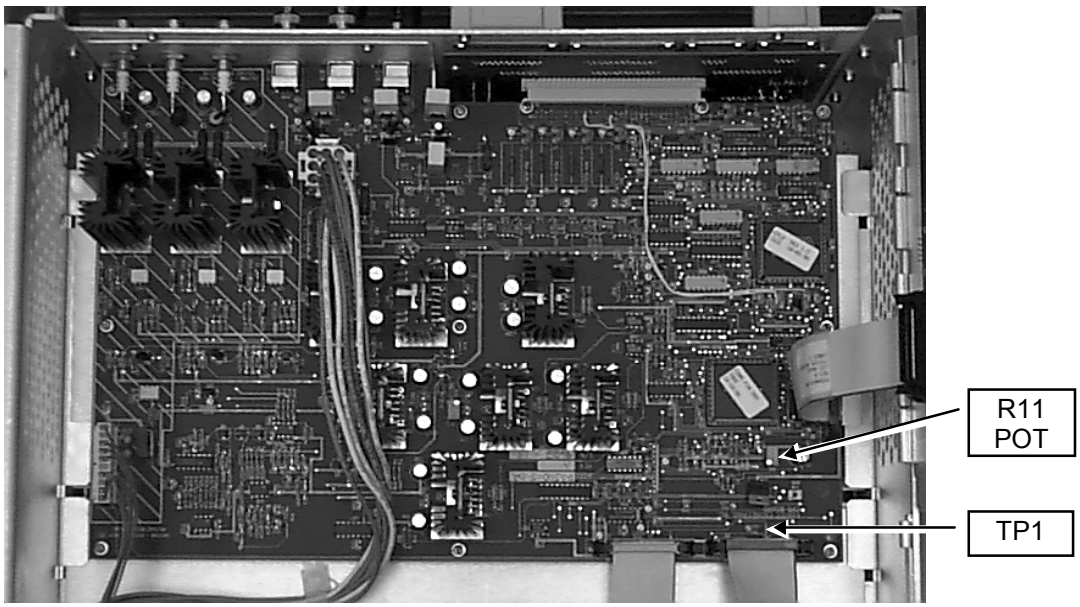
Verify that the cables are properly connected (not swapped) at J20 (Multi-Coil Signals, labeled MR1-A7-J20) and J18 (Multi-coil TR Bias, labeled MR1-A7-J18); see Illustration 7-2.



CABLES CONNECTED TO CORRECT LOCATIONS — MULTI-COIL
ILLUSTRATION 7-2

7-1-1 Via the Front Panel Switches (continued)

1. Connect an oscilloscope or a Digital Volt-Meter to the CPD Board test point TP1 (–5VDC) with reference to ground; see Illustration 7-3. Adjust R11 until the voltage measured is –5.00 VDC (± 0.05 VDC).



MULTI-COIL ADJUSTMENT/ –5VDC AT TP1
ILLUSTRATION 7-3

8- PAC VOLTAGE CONFIGURATION

The PAC is preset to 9 VDC at the factory (setting should be verified if the spare board seal is broken).

The PAC Voltage can be verified via an alternate proprietary GE procedure or Via the Front Panel Switches using Section 8-1.

Note

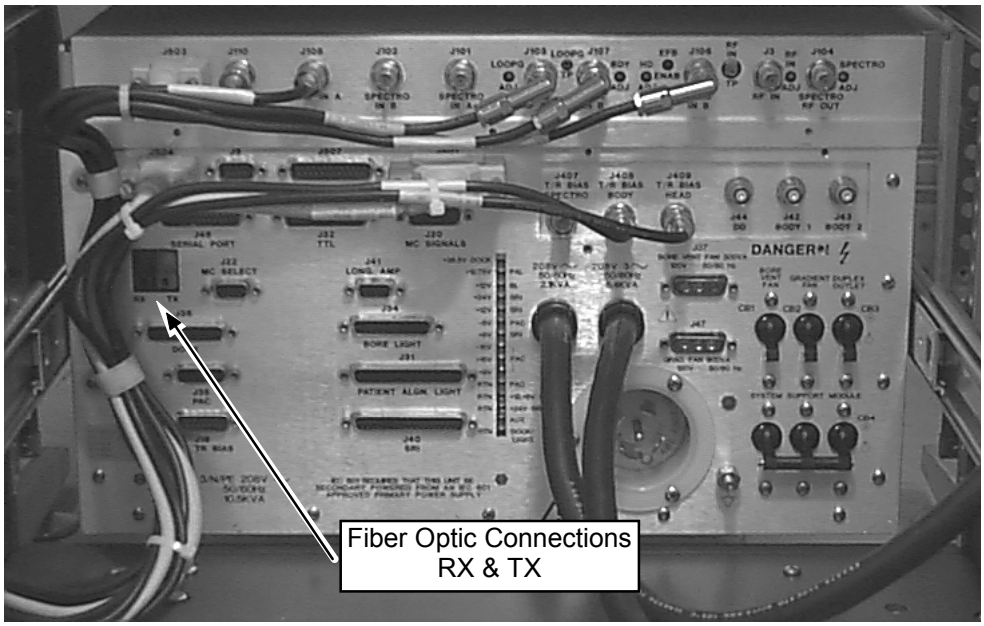
Systems without a fiber optic repeater at the Pen wall need to set the PAC voltage to 8 Volts DC.

CAUTION

Possible equipment damage. To prevent possible damage to equipment due to incorrect voltage settings, systems without fiber optic repeater at the Pen wall need to set the PAC voltage to 8 Volts DC.

8-1 Via the Front Panel Switches

1. Remove Fiber Optic cables from rear of SSM (RX & TX). See Illustration 8-1.



FIBER OPTIC CABLE CONNECTIONS
ILLUSTRATION 8-1

2. Remove the plastic cover on the front of the SSM.

Note

Place DIP Switch #1 in the UP position last. Order of DIP switch placement is important otherwise system will not recognize changes.

3. To change the PAC voltage setting, perform one of the following steps:

8-1 Via the Front Panel Switches (continued)

a. **For systems without the fiber optic repeater, set to 8 VDC**. Place switch 6 in the Down position and switches 4 & 1 in the UP position. Ensure that all other switches are in the Down position.

   Verify system is recognizing change by the LED display; Bank 1 LEDs 1, 2, & 5 will be illuminated.

b. **For systems with the fiber optic repeater, set to 9 VDC**, place switches 6, 4, and 1 in the UP position.

   Verify system is recognizing change by the LED display; Bank 1 LEDs 1, 3, & 5 will be illuminated.

4. Place switch 1 in the Down position.

5. Place all other switches in the Down position.

6. Cycle the main breaker power at the SSM by turning CB4 to the OFF position, waiting 15 seconds, then setting CB4 to the ON position. This step saves the changes to the SSM.

7. Replace the plastic cover on the front of the SSM.

8. Connect the Fiber Optic cables to RX & TX on rear of SSM.

9. Perform TPS Reset by clicking the **[Service Desktop]** icon and clicking the **[TPS Reset]** button on the Service Rx.

9- POWER MONITOR TYPE CONFIGURATION

The power monitor should be checked to verify that it is set to either 1.5T or 1.0T, depending on the field strength of the system. The default setting for replacement boards is 1.5T. The power monitor type can be changed one of two ways: an alternate proprietary GE procedure or via the front panel switches (Section 9-1).

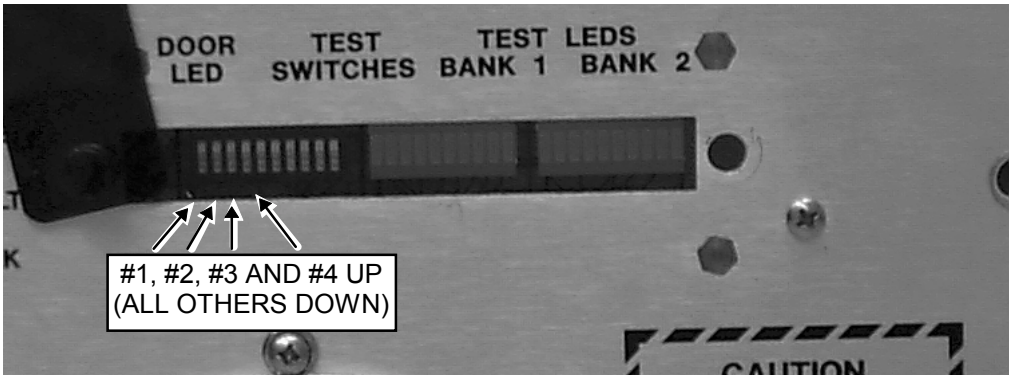
9-1 Via the Front Panel Switches

1. Remove the plastic cover on the front of the SSM.

Note

Place DIP Switch #1 in the UP position last. Order of DIP switch placement is important otherwise system will not recognize changes.

2. Place switches 3, 2, 4, and 1 in the Up position. Ensure that all other switches are in the Down position (See Illustration 9-1). Depending on the current configuration of the Power Monitor LED BANK 1 and LED BANK 2 will each show either LED # 2, LED # 3, or LED # 4 illuminated. LED # 2 illuminated signifies a 1.0T, LED # 3 illuminated signifies a 0.7T, and LED # 4 illuminated signifies a 1.5T Power Monitor. It is not necessary to continue this procedure if the Power Monitor is already correctly configured.



DIP SWITCH CONFIGURATION FOR SETTING POWER MONITOR TYPE
ILLUSTRATION 9-1

a. **To set the type to a 1.0T**, place switch 5 in the Up position and switch 6 in the Down position.

b. **To set the type to a 1.5T**, place switch 5 in the Up position and switch 6 in the Up position.

3. Place switch #10 in the Up position followed by the Down position. LED BANK 1 and LED BANK 2 will now change to show either LED # 2 (1.0T) or LED # 4 (1.5T) illuminated depending on the new setting of the Power Monitor.

4. Place switch #1 in the Down position. None of the LEDs in LED BANK 1 and LED BANK 2 should now be illuminated.

5. Place all other switches in the Down position.

6. Cycle the main breaker power at the SSM by turning CB4 to the OFF position, waiting 15 seconds, then setting CB4 to the ON position. This step saves the changes to the SSM.

9-1 Via the Front Panel Switches (Continued)

7. Replace the plastic cover on the front of the SSM.

10 - SYSTEM RESTORATION

1. Close the SSM lids, replace all the lid screws, slide the SSM chassis back into the rack, and replace the four front screws.

2. Remove Laptop computer connection to SSM (J46), if applicable.

3. Replace cabinet covers.

4. Verify J5 is connected.

5. Perform a TPS reset.

6. Perform a Head Scan, Body Scan, and Multi-coil scan to verify the system is scanning normally.

REVISION HISTORY

REV	DATE	AUTHOR	PRIMARY REASONS FOR CHANGE
0	July 25, 1997	Karyl Verdon (Erbtec)	Initial Release - checked consistency w/existing files.
1	June 29, 1998	K. Keshena	Updated file to RF/PDU cabinet
2	December 28, 1998	K. Keshena	Added alternate proprietary procedure information, updated laptop portion to Windows95, and corrected switch orders for the front panel switch procedures.
3	January 25, 1999	R. Lambert & K. Keshena	Combined procedures, this procedure is for RF/PEN II and 1.0T & 1.5T RF/PDU systems. Clarified all sections.
4	November 16, 1999	R. Schmidt	Updated page 17 with correct path for loading CPD.exe program as well as latest CD-ROM part #'s for 5x & 8.x. Page 18 steps 7-2-2, 7-2-2-b, & 7-2-4 were validated and corrected per SPR's MRIge56704 & MRIge56649 in which LED 4 is illuminated, not LED 2.
5	October 6, 2000	D. Thome'	Added new Warning message about disconnected bias lines. Added reference to SRF cabinet. Corrected section 6-2 concerning LEDs and section 6-1-1 concerning multi-coil switch setup. Added TR waveforms for head and body. Re-wrote procedures for class A.
6	March 12, 2001	D. Thome'	Added reference to 0.7T Power Monitor configuration information. Added notes and comments to clarify calibration procedure.
7	March 22, 2001	D. Thome'	Added Section 3 to check JP1 on HV Board.